MTP-M-G&C-61-1
March 10, 1961

GEORGE C. MARSHALL SPACE FLIGHT CENTER

HUNTSVILLE, ALABAMA

FINAL ENGINEERING REPORT
SATELLITE S-45 INOSPHERE BEACON TRANSMITTER
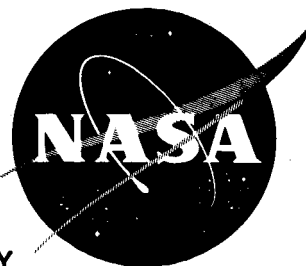
By

Alan J. Fisher

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

GEORGE C. MARSHALL SPACE FLIGHT CENTER

MTP-M-G&C-61-16

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ABSTRACT

This report covers the design and construction of a six frequency
radio transmitter. Its function is to make possible measurements of
the upper ionosphere with an artificial earth satellite. The
transmitter develops for radiation the 20th, 40th, 41st, 108th, 360th,
and 960th harmonics of a stable one megacycle quartz crystal oscillator.
An overall efficiency of 30% is accomplished by the use of high
efficiency capacity diode frequency multipliers and transistor amplifiers.
The design also features a unique thermal null filter which eliminates
crystal temperature changes at the orbit frequency so that great
frequency stability is obtained without a crystal oven.

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RF SYSTEMS DEVELOPMENT SECTION
INSTRUMENTATION DEVELOPMENT BRANCH
GUIDANCE AND CONTROL DIVISION

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I. INTRODUCTION

A. General

On September 29, 1958, the National Bureau of Standards sponsored an ionosphere measurements meeting in Boulder, Colorado. The representatives present agreed that a satellite specifically designed to radiate signals suitable for making measurement of the upper ionosphere by Faraday rotation of polarization would be of great interest and benefit. In January 1959, the Missile Instrumentation Development Branch of the Army Ballistic Missile Agency released ABMA Report No. DG-TM-3-59, Proposed Ionosphere Satellite, by Alan J. Fisher. As a result of this report and other information exchanged, ABMA was given funds by the National Aeronautics and Space Agency (NASA) to develop and launch such a satellite.

This report deals only with the development and realization of the radio frequency transmitter for this satellite. This development program was begun in May 1959 and after a few interruptions and delays, it was essentially completed in October 1960 with the construction of three prototypes, the flight, and spare flight models. In this period, the project was carried on by Alan J. Fisher with the assistance of Mr. William Bennett, electronics development technician. During the project, the Development Operations Division of ABMA (including personnel working on this project) was transferred to NASA. All of the design and construction of this transmitter was done in the Instrumentation Development Branch of Guidance and Control Division, now of Marshall Space Flight Center, NASA.

B. Need

The ionosphere is the electrified region that exists in the upper atmosphere above approximately 50 km. It affects radio communication in many different ways. At low frequencies it acts like a reflector, at medium frequencies it partially reflects and partially absorbs radio energy. At still higher frequencies energy may pass through with no effect other than a twisting or rotation of the radio field. The ionosphere appears to consist of several layers which have different radio characteristics that change from day to night and also change with sun spot activity. The multiple layer structure is sometimes approximated by a single layer whose intense cross section with altitude is parabolic so that the uncertain upper half of the layer is an extrapolation of the lower half. This parabolic model is useful in considering the twisting or Faraday rotation of radio signals passing through the ionosphere.

Studies of the Faraday rotation of lunar radio echoes indicate that the total electron content at night is more than twice that of a simple parabolic layer. This suggests that during the night there are more than three times as many electrons above the altitude of maximum intensity as below. Ionosphere structure below the maximum is available from extensive vertical-incidence radio soundings made during the International Geophysical Year. Above the maximum, details of the ionosphere structure are obscured for soundings from below, and are not provided from lunar echoes since they reveal only the integrated ion content over the earth-moon path. Therefore, the structure of the greater portion of the ionosphere above the maximum is not known. By placing sources of radio energy at appropriate frequencies and at various positions in the ionosphere, much added information about the structure will be obtained from ground radio receiving sites. This is to be accomplished by placing the subject radio transmitter in an artificial earth satellite ranging in altitude from 200 to 1400 miles so that this multiple signal source will be carried throughout the upper ionosphere. Field strength recordings from the EXPLORERS and SPUTNIKS have shown the feasibility of such an experiment, but the signals and orbits of these satellites were not particularly suited to this purpose. Therefore, a satellite transmitter specifically designed to probe the ionosphere has been developed and that effort is reported here.

C. Target Characteristics

At the outset of the development program the target characteristics for the beacon were:

1. Outputs

Six radio frequency outputs all harmonically derived from a single 1.00025 mc oscillator so that their phase relations are coherent.

(a) 20th harmonic output of 300 mw

(b) 40th harmonic output of 100 mw

(c) 41st harmonic output of 100 mw

(d) 108th harmonic output of 20 mw and phase modulated with telemetry

(e) 360th harmonic output of 100 mw

(f) 960th harmonic output of 10 mw

2. Frequency Stability

The frequency stability of the basic oscillator and hence of all output frequencies needs to be at least one part in ten to the seventh power during any half hour period (approximate time the satellite will be in radio view of a given receiving site).

3. Power Consumption

The transmitter will have available to it between 2 and 2½ watts with which to generate the outputs, i.e. an overall efficiency of about 30%.

4. Environment

The transmitter must operate in the vacuum and temperature extremes of space and endure the vibrations and shocks of launching and injection into orbit. The environmental tests reported in part IV of this report will specifically indicate these requirements.

II. DESIGN

A. Thermal Design

In order to provide a frequency stability of one part in ten to the seventh power per half hour period, the basic oscillator employs a quartz crystal with minimum frequency change with temperature. Time rate of frequency change is critical rather than maintaining absolute frequency. Therefore the frequency may change, providing it does so very slowly. With the requirement of about 30% overall electrical efficiency, it is impossible to use any of the power available to power a crystal oven to maintain constant crystal temperature. Thus, the approach taken was one of building a passive thermal filter around the oscillator which would allow only very slow temperature changes to occur at the crystal. For example, the crystal may be placed along with material of high heat capacity inside a jacket of insulating material with high thermal resistance. The thermal "RC" time constant of these materials will prevent rapid temperature changes of the crystal because they act as an integrating filter. One difficulty with this approach is that electrical conductors usually must bridge the insulation to external circuits and thus thermally short-circuit the insulation to some extent. A design has been made which takes advantage of the heat conducted by these electrical conductors to provide an attenuation to periodic temperature changes much greater than possible, even with no conductors.

When a thermal low pass filter is made with lumped heat capacity and insulation, the maximum phase shift to periodic temperature changes will be less than 90° as with a simple series R, shunt C, single section electrical filter. However, if the crystal is surrounded with a sphere of homogeneous material that possesses low thermal diffusivity, a much greater phase shift to periodic temperature changes may occur. Such an arrangement and its elect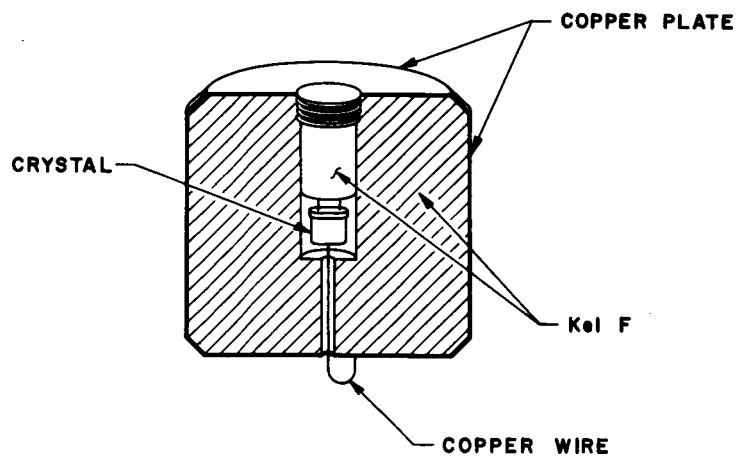rical analog are shown in Figure 1. Each of the cascaded series R, shunt C, filter sections represents diffusion of heat through an incremental radial distance in the sphere. For a given sphere there will be a frequency at which the heat flow into and out of the crystal is lagging the outside heat flow by one-half cycle. Under these conditions, if a second heat path is added which has the same attenuation as the sphere but no delay, cancellation of heat flow will occur at the crystal to allow the crystal to remain at a constant temperature. This added heat path may be a filament of material with a heat diffusion rate that is very high compared to the material of the sphere. A metal wire(or wires) is appropriate as it can also serve to make electrical connections to the sphere's interior. Thus, we may visualize a sphere of material with low thermal diffusivity which has a metallic outer shell to assure an isotherm on the outside, a smaller metal sphere at the center (which contains the crystal) and a metal wire connecting the two metal spheres (see Figure 1). If both heat paths are properly proportioned, as the inter-shell is receiving heat that started propagating through the low diffusivity material a half cycle earlier, it is having exactly the same amount of heat removed through the metal wire by the cool half cycle now occurring at the outer shell. Thus, there is no net heat flow to the crystal and it remains at a constant temperature providing the outside temperature is varying at a single frequency. Satellite temperature variations are not strictly of this type, but nevertheless an analysis of satellite temperature variations will show the frequency spectrum to have an outstanding component at the orbit frequency. A crystal thermal capsule of the type described can eliminate this strongest component of the spectrum and therefore, solve the major part of the problem. Lower frequency components are not too serious since they have a slower time rate of change and higher frequency components may be easily filtered out with more simple insulation techniques.

The design objective was to provide the thermal null at a frequency of 0.50 cycles per hour (120 min. orbit). One need not consider much farther to realize that the evaluation of such a device would be most time consuming since a few cycles at each test frequency would have to precede the data collection to eliminate all starting transients. For this reason a great deal of study of effects was first done with an electrical analog model. Frequency responses, phase shifts, and proportions of conductances and capacities were studied with this model so that experience in adjusting for a perfect null and interpreting indications could be gained rapidly. Next a

THERMAL MODEL   ELECTRICAL MODEL

DELAYED HEAT PATH

DIRECT PATH

DELAYED PATH

T_{OUT}

T_{IN}

$E \alpha T_{OUT}$

$E \alpha T_{IN}$ $I = 0$

METAL SPHERES

DIRECT HEAT PATH
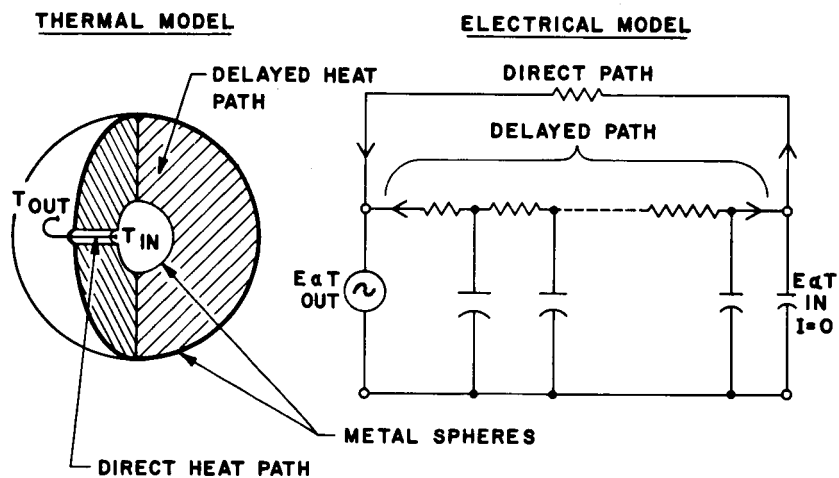
ENVISIONED THERMAL MODEL AND ELECTRICAL ANALOG

Fig. 1

COPPER PLATE

CRYSTAL

Kel F

COPPER WIRE

FORM OF ACTUAL THERMAL CAPSULE

Fig. 2

thermal model was built. A search for low diffusivity (low thermal conductance and high specific heat) materials narrowed down to two plastics: regenerated cellulose and Kel-F. Although the cellulose would have weighed less and been smaller, Kel-F was chosen because it is relatively easier to fabricate and does not contain matter that will out-gas in the vacuum of space. Because of the shape of the crystal holder and for ease of fabrication, the Kel-F was machined with cylindrical instead of spherical geometry. The outer surface of the Kel-F cylinder was plated with 10 to 15 thousandths of an inch of copper to establish an isotherm. The metal crystal holder served as the interisotherm. This construction is shown in Figure 2 and in Figure 3. The central cavity contains the crystal and transistor oscillator circuit. These are potted in silicon rubber so that when the Kel-F plug of Figure 3 is screwed down, the rubber is forced into intimate thermal contact with the Kel-F and crystal for a reproducible heat diffusion path in a vacuum environment. As it happened, the signal and power conductors to the oscillator did not conduct suffi-cient heat to obtain the null so they simply ran parallel to the larger copper wire shown soldered to the crystal can and outer plating in Figure 2. The cylinder is 4.78 inches in diameter and in length for a null at 0.50 cycles per hour. The copper plating on the Kel-F is buffed to a mirror finish and gold plated for low thermal emissivity. This cylinder is then supported by suitable Kel-F pieces inside a larger outer canister that has polished gold surfaces inside and out (see Figure 4). This combination forms a thermal bottle with space supplied vacuum. The void between the canister and Kel-F cylinder contains fourteen printed circuit boards arranged like spokes of a wheel; these help support the Kel-F cylinder. These boards carry the solid state amplifiers and harmonic generators which develop the six frequencies (Fig. 5). Two ridges on the sides of the thermal capsule space the boards from it to minimize heat conduction. The access holes in the canister are for adjusting the circuits and they also allow the ,air to escape from the thermal-bottle type structure. This additional vacuum insulation suppresses harmonics of the orbit frequency temperature changes so that a radio frequency stability of one part in ten to the tenth (.002°C change) per orbit would result if it were not for circuit noise and voltage variations.

In order to evaluate the design, extremely small internal tempera-ture changes had to be measured. This was done by choosing a quartz crystal with a particularly high rate of motional frequency change with temperature and by calibrating its oscillating frequency versus tempera-ture. By the use of precision frequency measuring equipment, a fre-quency change of 1 part in 10^9 may be measured which correspond to about five ten-thousandths of a degree centigrade change in crystal temperature. The remaining problem in evaluation was that of establish-ing a sine wave of temperature with constant amplitude and frequency on
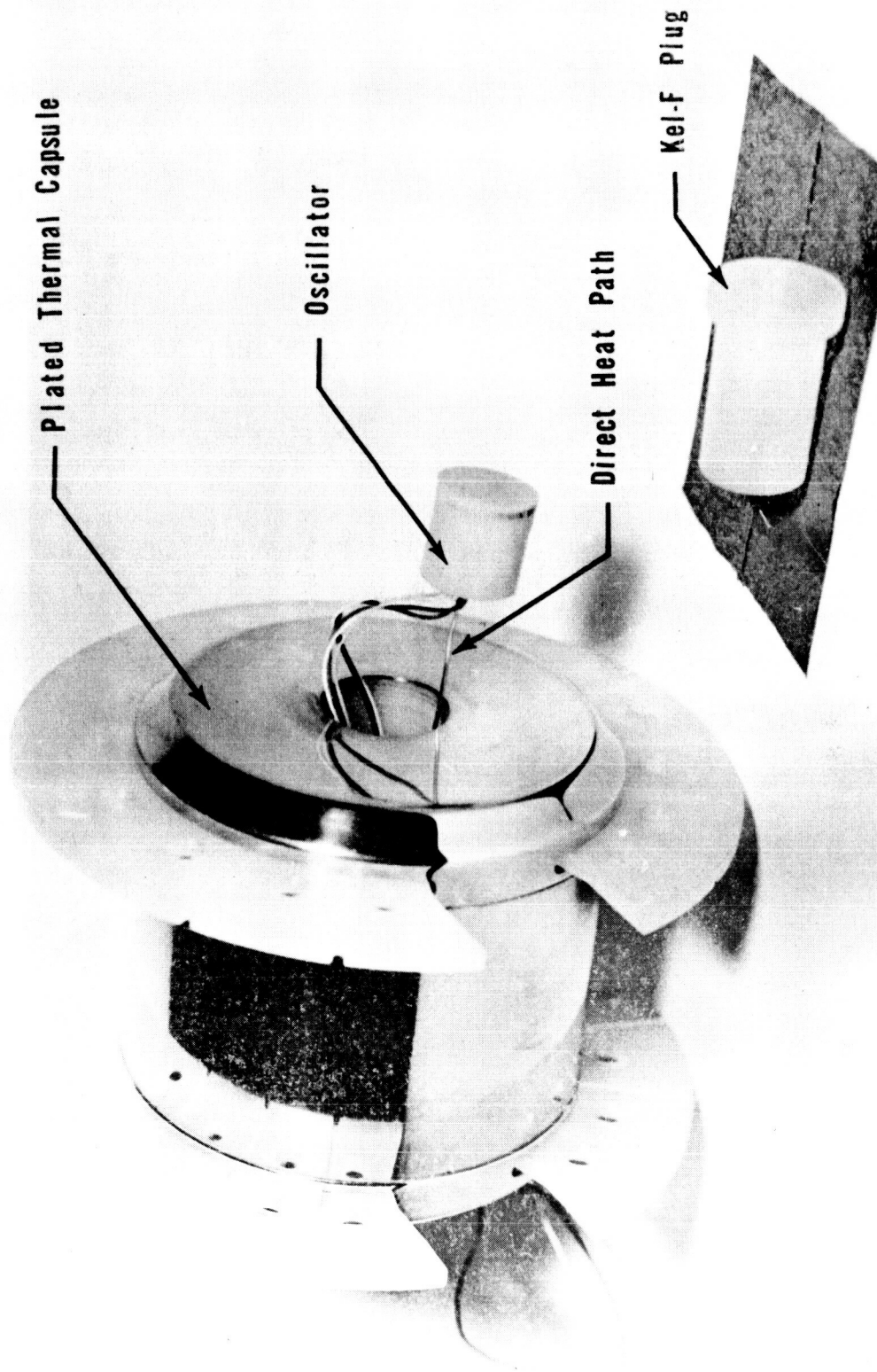
PARTS OF THERMAL CAPSULE DISASSEMBLED

Fig. 3

Lid

Compression
Sleeve

Heat Sink
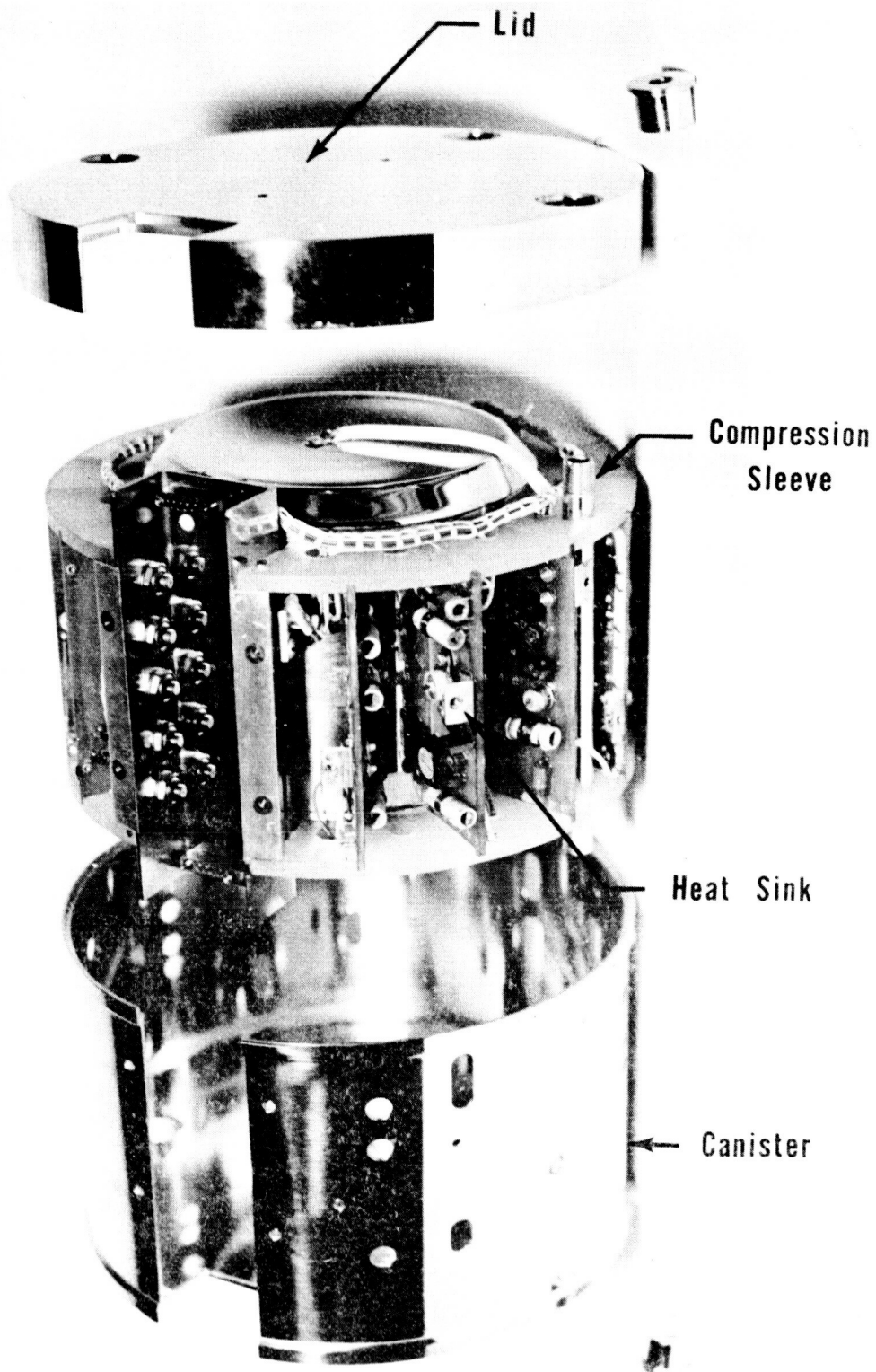
Canister

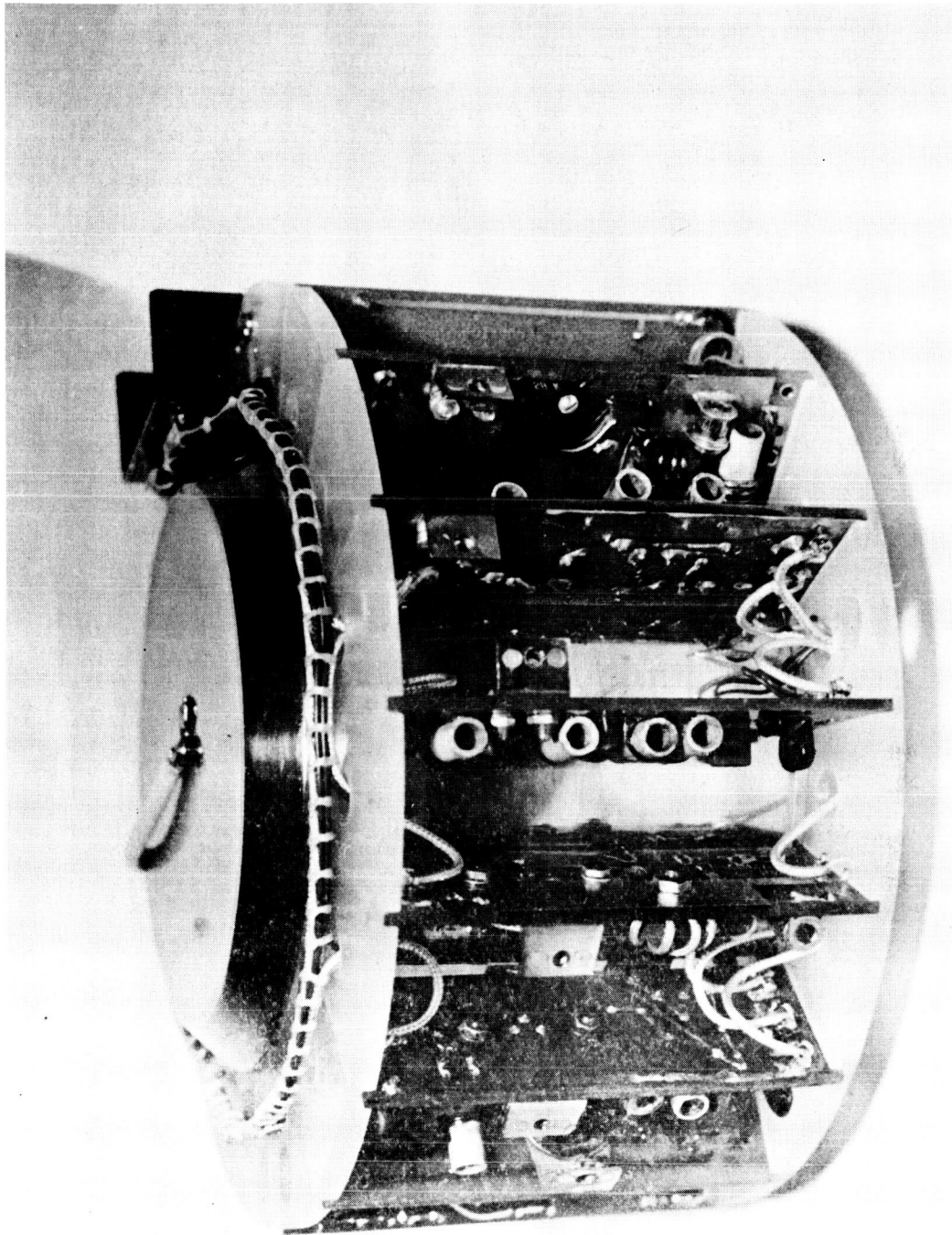**Exploded View Of Beacon Deck**   **Fig. 4**

FIG. 5 BEACON WITHOUT CANISTER

the outside plating. This was accomplished by manually switching a temperature chamber from hot to cold at the desired frequency and putting insulation around the thermal capsule so that the steps in temperature would be filtered into nearly a sine wave when they arrived at the capsule. Figure 6 is a plot of the frequency response of the electrical analog model and it shows the deep null produced by the addition of the direct path. The circles are data collected from the thermal model. The lower curve shows the thermal frequency response of the entire assembly including the insulation of the vacuum gap. All of this data, except for the circles, was obtained from the electrical analog.

Figure 7 shows the electrical analog circuit and scaling factors used. Included here are the analog components for the rest of the payload heat transfer between the payload skin and centrally located crystal oscillator. This includes another vacuum gap between the instrument column and the rest of the satellite and the heat capacity of the instrument column (not including the thermal capsule since it is represented by itself in the analog circuit). Figure 8 shows some step function responses of this analog circuit labeled in time scaled to the heat transfer case. The early hump seen in the response of the capsule analog, Figure 8a, is due to flow conducted by the direct path. Figure 8f shows that the overall payload time constant to the 50% temperature change point is 16.4 hours by the analog. A thermal balance test of the actual payload indicated 16 hours. This same test indicated a time constant of 3.75 hours from payload skin to the canister compared to the 4 hours in Figure 8d for the analog. From these and other checks, it is felt that the analog is a very good representation of the actual case. The major exception seems to be a second order one; the fact that in the electrical analog the transfer components for the vacuum gaps are linear while in the thermal case they are not, since the heat transfer is by radiation.

B. Structural Design

The complete Kel-F thermal capsule weighs 7.1 pounds and is supported by the two Kel-F "C" shaped rings and fourteen printed circuit boards. The rings fit into slots in the Kel-F cylinder and the circuit boards fit into slots in the rings. The diagonal strength of the circuit boards prevents the two rings from diaphragming under the force of launch acceleration on the mass of the crystal capsule. The rings rest on ledges in the canister and lid, so that the rings and circuit boards are put into compression when the three compression sleeves are tightened on the complete assembly. These parts may be seen in Figures 3 and 4 and in the assembly drawing of Figure 9. The lip at the outside bottom of the canister and plain edge at the top of the lid (Figure 10) align the beacon with other similarly constructed instrument decks when they are stacked like dishes. Two rods then pass
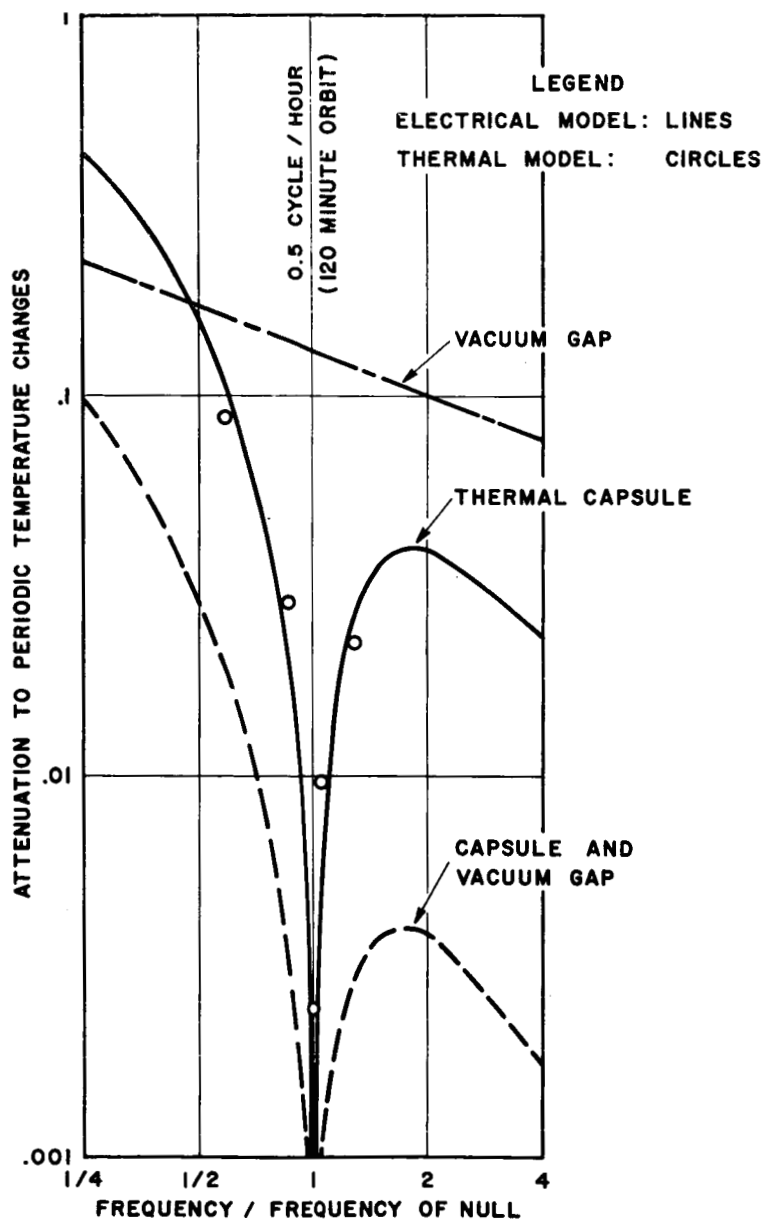
FIG. 6 FREQUENCY RESPONSE OF THERMAL
DESIGN AND ELECTRICAL ANALOG

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FIG. 7 ELECTRICAL ANALOG FOR PAYLOAD HEAT TRANSFER IN S-45
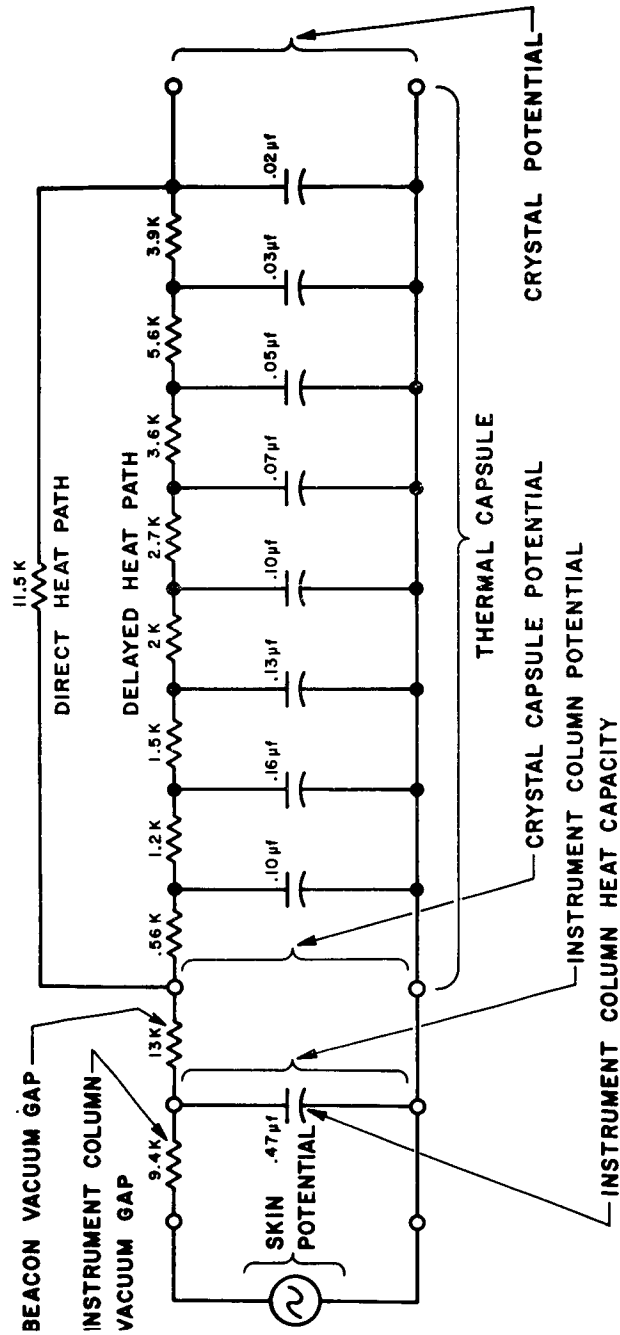
ANALOG EQUIVALENTS:

ELECTRICAL		THERMAL	
.001 SEC	=	1 HOUR	(TIME)
1 OHM	=	$835 / \frac{K-CAL}{HR \cdot ^\circ C}$	(RESISTANCE)
1 FARAD	=	$\frac{K-CAL}{^\circ C} / 835,000$	(CAPACITY)
1 VOLT	=	$1 ^\circ C$	(POTENTIAL)

(a) 50% ... 0 ... 0 1 2 3 4 5 HOURS — CAPSULE SURFACE TO CRYSTAL
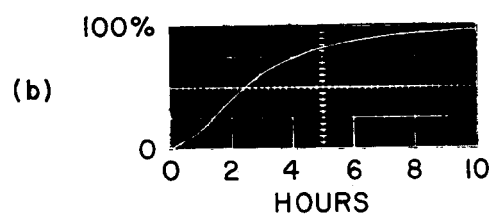
(b) 100% ... 0 ... 0 2 4 6 8 10 HOURS — CAPSULE SURFACE TO CRYSTAL (DIFFERENT SCALE)
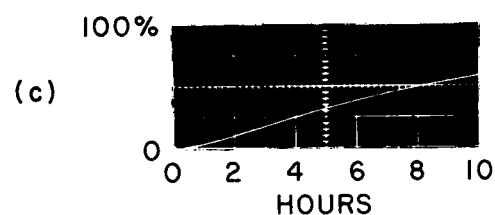
(c) 100% ... 0 ... 0 2 4 6 8 10 HOURS — CANISTER TO CRYSTAL (CAPSULE + VACUUM GAP)
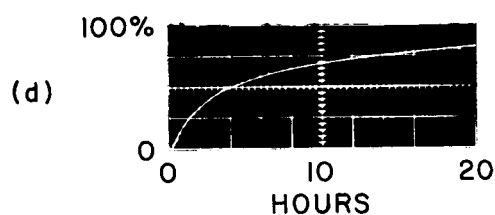
(d) 100% ... 0 ... 0 10 20 HOURS — PAYLOAD SKIN TO CANISTER (INSTRUMENT COLUMN VACUUM GAP)
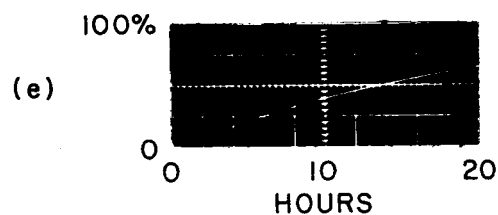
(e) 100% ... 0 ... 0 10 20 HOURS — PAYLOAD SKIN TO CAPSULE (BOTH VACUUM GAPS)
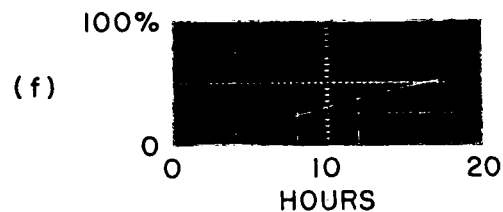
(f) 100% ... 0 ... 0 10 20 HOURS — PAYLOAD SKIN TO CRYSTAL (BOTH VACUUM GAPS AND CAPSULE)

FIG. 8 PAYLOAD STEP FUNCTION TEMPERATURE RESPONSES
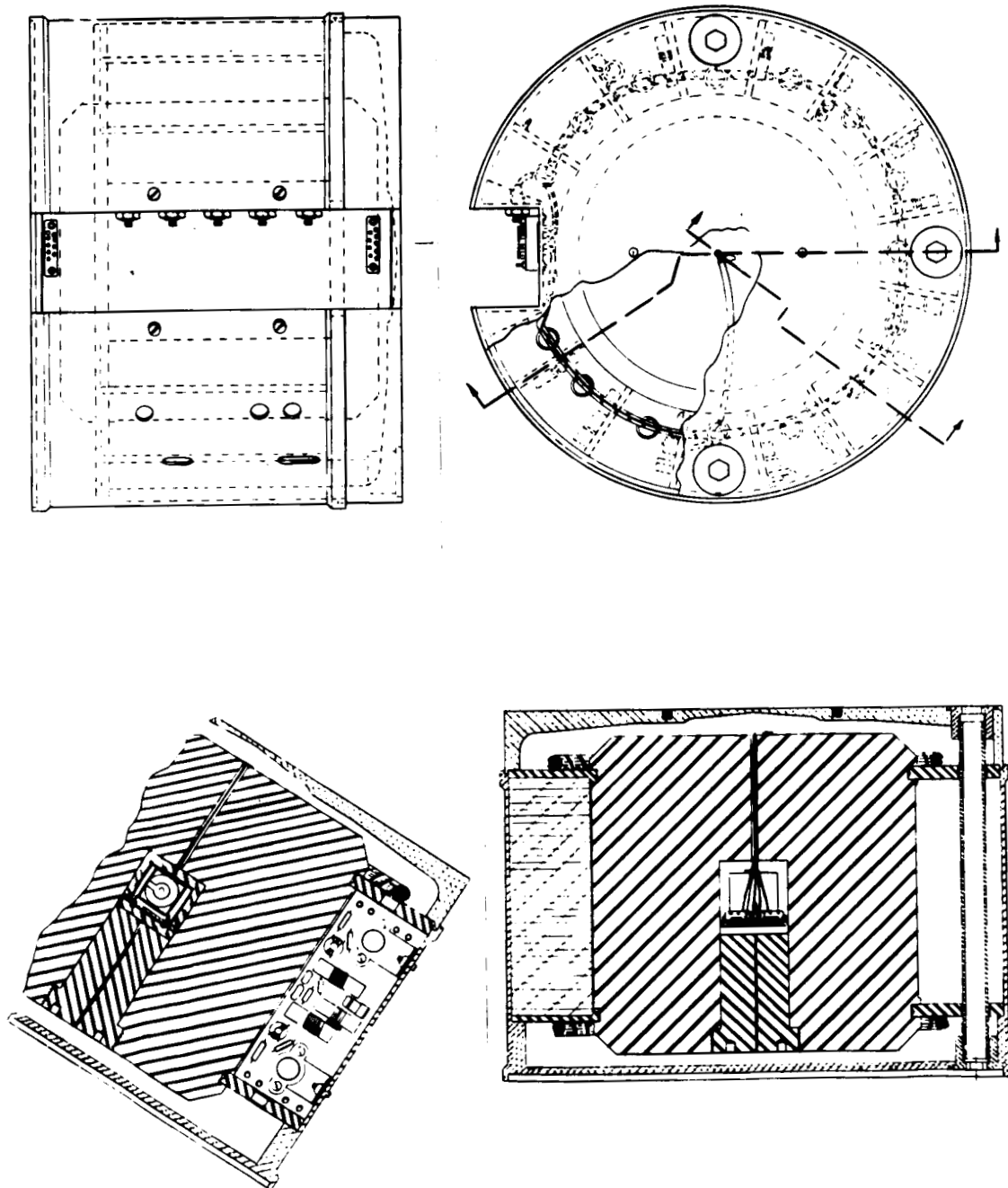
FIG. 9   ASSEMBLY DETAILS
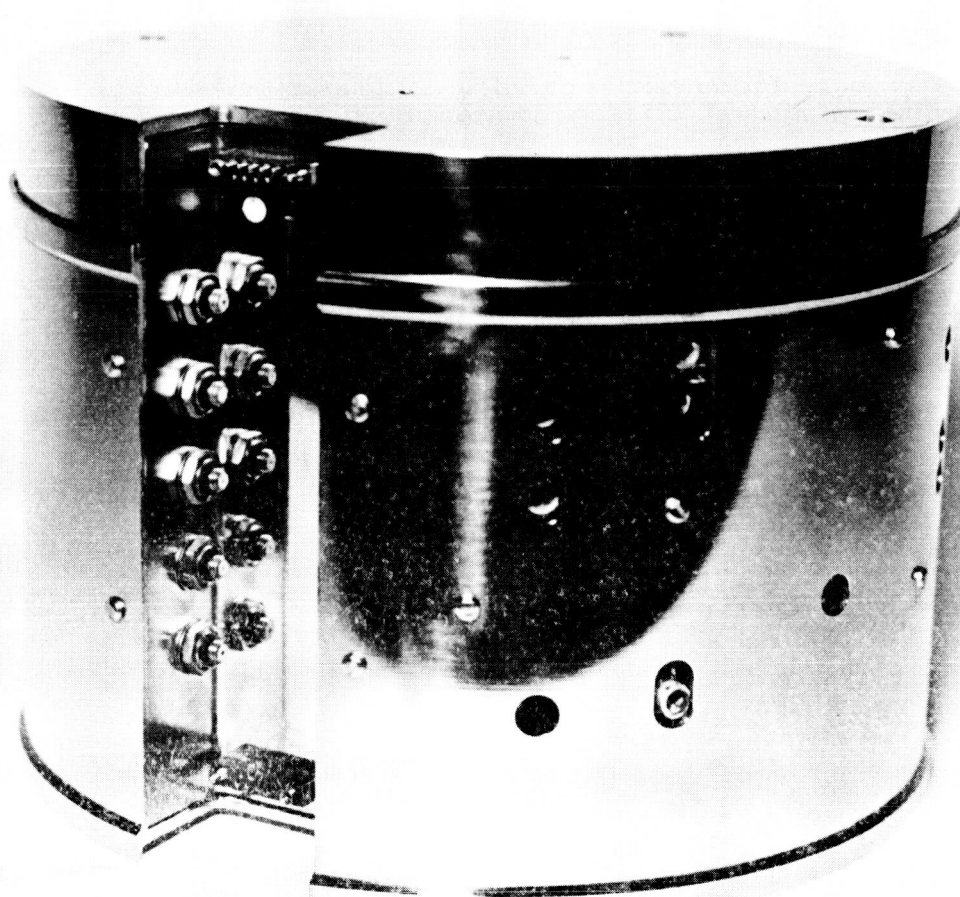
FIG. 10   COMPLETE BEACON DECK

through the diametrically opposite compression sleeves to align the
wiring channels in all of the decks in the payload instrument column.
All electronic parts in the beacon are ruggedized by fillets of
Armstrong C-1 compound with 40% flex added. All screws are secured
either by locking devices or with cement.

C. Electronics Design

In order to keep the power supply required by the beacon to a
single voltage, it was decided to use transistors throughout the equip-
ment. A single voltage solar cell and storage battery system can
produce more power than a multiple voltage supply for a given available
area of solar cells. With the requirement of an overall efficiency of
about 30%, it was necessary, wherever possible, to operate transistor
power amplifiers at zero bias so that the power usually lost in
stabilizing bias networks could be saved. This resulted in the output
power of these amplifiers dropping off when they got cold because of the
increase in their emitter-base contact potential which acts like a class
"C" bias. This effect was partially overcome by causing the drive
voltage to these stages to increase when cold. This type of biasing
also caused a threshold effect in the gain of the stages so that the
drive had to be kept quite constant as supply voltage changed.
Wherever practical, the input and output impedances of the sections of
the beacon were made to be 50 ohms. This simplified testing and
evaluation of each section, and also made it easier to employ portions
of this design in other equipments, should the need arise. In order to
achieve the required 30% overall efficiency, the highest possible
efficiency was sought throughout the design. This resulted in the use
of several state of the art advances in transistors, capacity diodes,
and circuit techniques for which no experience and reliability data
existed. For this reason, considerable care has been exercised to over-
test these features to assure a reasonable degree of reliability. The
scheme of the electrical design can be best understood by a quick
signal tour through the beacon.

Figure 11 is a composite signal flow diagram, block
diagram, and schematic circuit diagram. Each separate printed
circuit board is indicated by a dashed line square. The signal flow
is from left to right starting at the basic oscillator. The
oscillator signal is amplified in the 1st harmonic amplifier and its
output is split three ways. The upper output (Figure 11) will be
followed later. The lower output goes to the test socket for test
purposes and terminates in an external 50 ohm load. The middle output
drives a 20 and 27th harmonic generator. The 27th harmonic is then
amplified in the lower part of the 20 and 27th harmonic limiters board
and hence drives the phase modulator and 27th harmonic amplifier board.
Its output is then multiplied by four in frequency (and phase shift) in
the 108th harmonic generator. This board delivers the 108th harmonic

SCHEMATIC WIRING DIA.
S45 IONOSPHERE
BEACON
TRANSMITTER

FIG. 11

TABLE OF PARTS FOR
SCHEMATIC WIRING DIAGRAM (Fig. 11)

C1	.001 mf	C31	.8-4.5 mmf	C61	.8-12 mmf
C2	.001 mf	C32	120 mmf	C62	12 mmf
C3	64 mmf	C33	180 mmf	C63	80 mmf
C4	64 mmf	C34	.01 mf	C64	12 mmf
C5	.01 mf	C35	.8-12 mmf	C65	12 mmf
C6	.01 mf	C36	.01 mf	C66	12 mmf
C7	270 mmf	C37	120 mmf	C67	80 mmf
C8	.01 mf	C38	200 mmf	C68	12 mmf
C9	.01 mf	C39	200 mmf	C69	1-6.5 mmf
C10	.01 mf	C40	.001 mf	C70	.01 mf
C11	.01 mf	C41	114 mmf	C71	48 mmf
C12	.47 mf	C42	.01 mf	C72	180 mmf
C13	680 mmf	C43	9 mmf	C73	22 mmf
C14	.01 mf	C44	.8-12 mmf	C74	.01 mf
C15	.001 mf	C45	.01 mf	C75	.01 mf
C16	.001 mf	C46	470 mmf	C76	12 mmf
C17	.8-4.5 mmf	C47	51 mmf	C77	4 mmf
C18	.8-4.5mmf	C48	18 mmf	C78	2 mmf
C19	250 mmf	C49	9 mmf	C79	.001 mf
C20	250 mmf	C50	.01 mf	C80	3 mmf
C21	180 mmf	C51	18 mmf	C81	2 mmf
C22	.001 mf	C52	12 mmf	C82	4 mmf
C23	390 mmf	C53	.8-12 mmf	C83	18 mmf
C24	390 mmf	C54	.8-4.5 mmf	C84	3 mmf
C25	.8-4.5 mmf	C55	.8-4.5 mmf	C85	.001 mf
C26	.01 mf	C56	64 mmf	C86	.6-1.8 mmf
C27	120 mmf	C57	.001 mf	C87	part of
C28	.001 mf	C58	5 mmf		PC745-B
C29	120 mmf	C59	40 mmf	C88	15 mmf
C30	180 mmf	C60	40 mmf	C89	.001 mf
				C90	2 mmf
				C91	.01 mf

TABLE OF PARTS
(Continued)

D1	11 volt zener		L20	11 turns, #30 wire, ¼" Dia.
D2	P.S.I. V100		L21	11 turns, #30 wire, ¼" Dia.
D3	P.S.I. PC-116-22		L22	9 turns, #24 wire, ¼" Dia.
D4	P.S.I. V100		L23	11 turns, #24 wire, ¼" Dia.
D5	P.S.I. V100		L24	3.3 uh
D6	P.S.I. V33		L25	5 turns, #24 wire, ¼" Dia.
D7	P.S.I. XC-120		L26	3½ turns, #21 wire, 5/32" Dia.
D8	P.S.I. XC-120		L27	4 turns, #20 wire, ¼" Dia.
D9	9 volt zener		L28	2 turns, #21 wire, 5/32" Dia.
D10	15.8 volt zener		L29	2¼ turns (C.T.), #18 wire, ¼"
D11	W.E. L2139		L30	4½ turns, #20 wire, ¼" Dia.
D12	P.S.I. PC-115-10		L31	2 turns, #16 wire, ¼" Dia.
D13	W.E. L2139		L32	6 turns, #21 wire, 5/32" Dia.
D14	P.S.I. PC-116-22		L33	8 turns, #30 wire, ¼" Dia.
			L34	9 turns, #30 wire, ¼" Dia.
L1	70 uh		L35	8 turns, #21 wire, 5/32" Dia.
L2	2.7 uh		L36	3 turns, #21 wire, 5/32" Dia.
L3	22 uh		L37	10 turns, #30 wire, ¼" Dia.
L4	4.7 uh			
L5	15 uh		PC	See printed circuit board
L6	14 turns, #30 wire, ¼" Dia.			drawings
L7	17 turns, #30 wire, ¼" Dia.			
L8	10 uh		Q1	Fairchild, X1040
L9	11 turns, #30 wire, ¼" Dia.		Q2	Fairchild, 2N699
L10	14 turns, #30 wire, ¼" Dia.		Q3	W.E. 2N1195
L11	6 turns, #30 wire, ¼" Dia.		Q4	W.E. 2N537
L12	7 turns, #30 wire, ¼" Dia.		Q5	W.E. 2N1195
L13	5 turns, #30 wire, ¼" Dia.		Q6	W.E. 2N1195
L14	5 turns, #21 wire, ¼" Dia.		Q7	W.E. GF40022
L15	2 turns, #21 wire, 5/32" Dia.		Q8	W.E. 2N537
L16	6.8 uh		Q9	W.E. GF40022
L17	21 turns, #30 wire, ¼" Dia.		Q10	W.E. 2N1195
L18	3.3 uh		Q11	W.E. 2N1195
L19	3½ turns, #18 wire, ¼" Dia.		Q12	W.E. GF40022

TABLE OF PARTS
(Continued)

R1	10K		R24	47K
R2	1.5K		R25	50K Pot.
R3	100		R26	3K
R4	15K		R27	10
R5	10K		R28	10K
R6	33K		R29	18K
R7	3.3K		R30	8.2K
R8	39K		R31	13K
R9	33K		R32	250 Pot.
R10	4.7K		R33	16K
R11	100		R34	16K
R12	39K		R35	20K Pot.
R13	5.6K		R36	16K
R14	560			
R15	1K Pot.		RT1	Crystal temperature thermistor 5K
R16	2.2K		RT2	Canister temperature thermistor 5K
R17	33K		RT3	50K thermistor
R18	220			
R19	1K Pot.		T1 thru T16	See transformer drawings
R20	6.8K			
R21	13K		TL	Transmission Line (part of PC745-B)
R22	10			
R23	10			

Y1	1.000250 mc, 1st mode, plated crystal, HC-6 holder
Y2	20.005 mc, 1st mode, plated crystal, HC-18 holder
Y3	27.00675 mc, 1st mode, plated crystal, HC-18 holder
Y4	20.005 mc, 1st mode, plated crystal, HC-18 holder
Y5	40.01000 mc, 3rd mode, plated crystal, HC-18 holder
Y6	41.01025 mc, 3rd mode, plated crystal, HC-18 holder
Y7	40.01000 mc, 3rd mode, plated crystal, HC-18 holder
Y8	41.01025 mc, 3rd mode, plated crystal, HC-18 holder

directly to the 108th harmonic antenna. The 20th harmonic output of the 20 and 27th harmonic generator is amplified in the upper part of the 20 and 27th harmonic limiters and hence drives the 20th harmonic amplifier. The power from this amplifier is also split three ways. The upper output drives the 40 and 41st harmonic generator which doubles the 20th harmonic to the 40th and sums this with the 1st harmonic to deliver the 40 and 41st harmonics. These signals then drive the 40 and 41st harmonic power amplifiers which supply their combined outputs to the 40 and 41st harmonic antenna. The middle output of the 20th harmonic amplifier drives the 20th harmonic power amplifier which supplies power to the 20th harmonic antenna. The lower output of the 20th harmonic amplifier drives the 120th harmonic generator which multiplies frequency by six to develop the 120th harmonic. This signal is amplified in the 120th harmonic power amplifier for drive to the 360th harmonic generator. This circuit multiplies by three to develop the 360th harmonic for that antenna and also multiplies by two to develop the 240th harmonic. This harmonic drives the 960th harmonic generator which multiplies by four to develop the 960th harmonic power for that antenna. The antennas may be seen in Figure 12. The six foot loop radiates the 20, 40, and 41st harmonics and the compound axial antenna radiates the remainder. Since most of these circuits are not conventional, some further discussion of each follows. Component nomenclature which follows refers to Figure 11, and the corresponding parts list Figure 11.

1. 1.00025 mc Oscillator

This circuit received a good deal of design time since it is the stable frequency source for all of the beacon's outputs. It is contained within the thermal capsule already described in part II, A. In order to keep the size and mass of the capsule as small as possible, the oscillator was made as small as possible. This size was determined by the smallest holder in which a 1 mc crystal could be obtained, an HC-6/U holder. This resulted in an oscillator which fits into a 1" x 1" right circular cylinder cavity in the center of the thermal capsule. The oscillator is shown in Figure 3 and without the silicone rubber incapsulation in Figure 13. An AT-cut, fundamental mode, plated crystal, was selected for the lowest possible frequency-temperature coefficient, shown in Figure 14. The physical constants of quartz cause this curve to be symmetrical about the temperature of $27^{O}C$. By cutting the quartz at slightly different angles, the temperature coefficient curve may be moved up or down. An angle of cut is selected which gives equal absolute coefficient at -3°, $+27^{O}$, and $+57^{O}C$. Allowing for thermal design errors, this $60^{O}C$ range should more than cover temperature changes occurring over long time periods as the ratio of direct sunlight to earth shadow changes. The thermal capsule cannot filter out these long term changes but instead filters out the per orbit temperature change of about $\pm 5^{O}C$ at the beacon canister. The attenuation of the thermal capsule to these changes is about 4×10^{-3} (Figure 6) and the vacuum gap between the capsule and canister adds about another 10^{-1} attenuation. Therefore, the
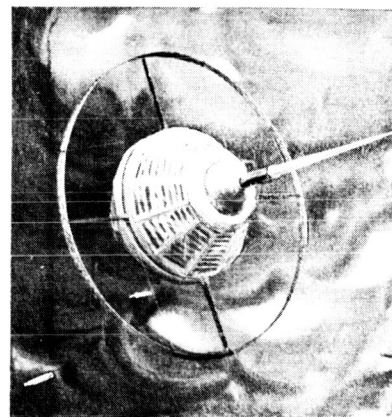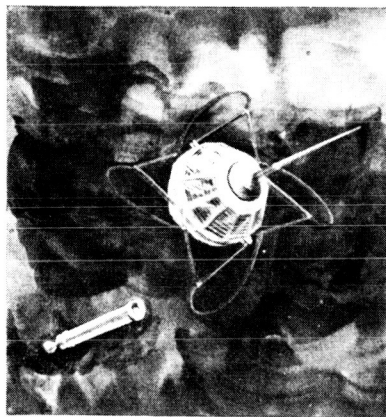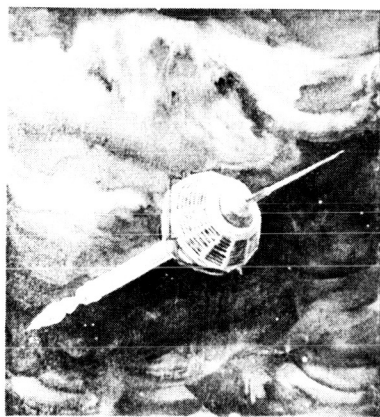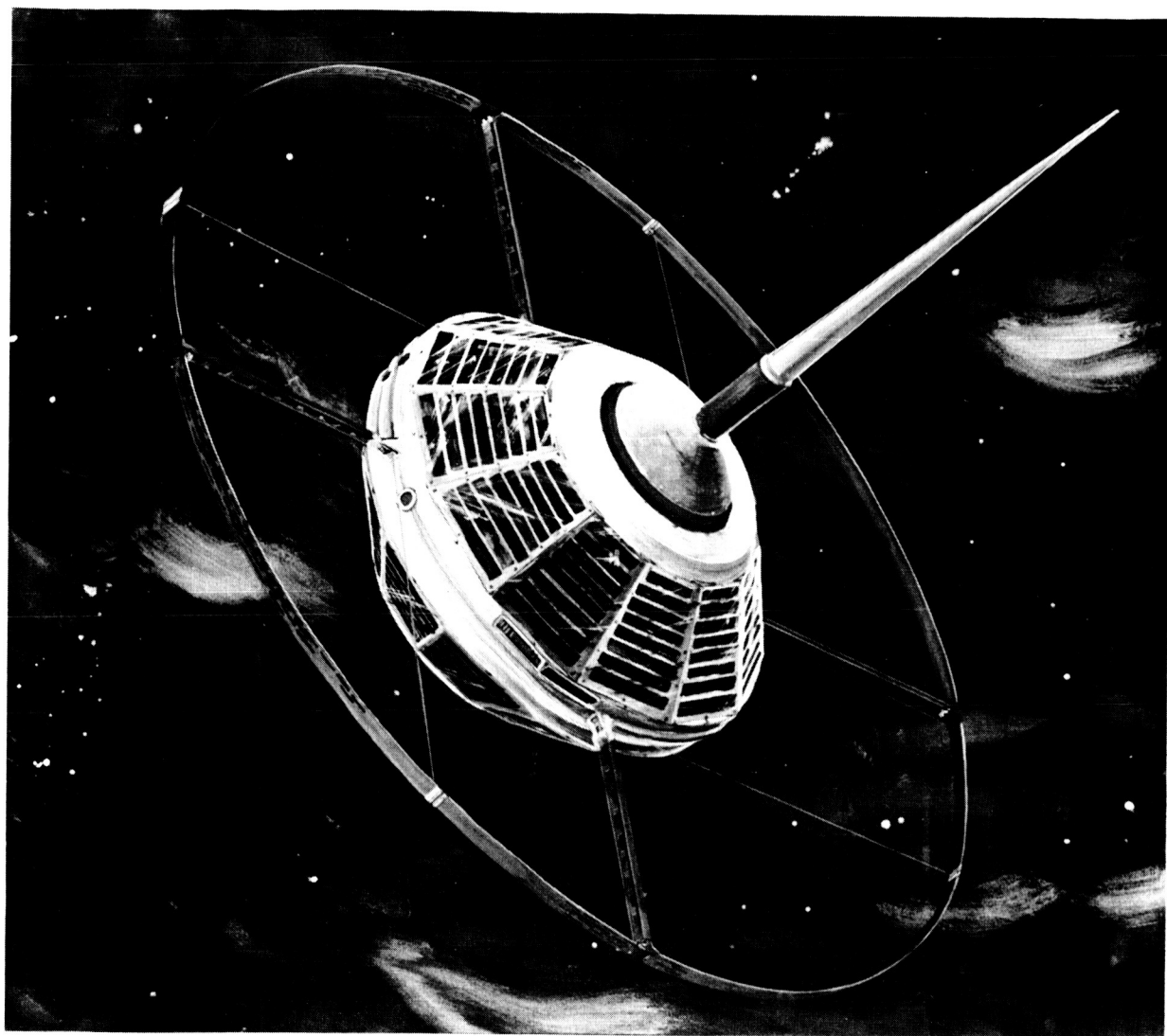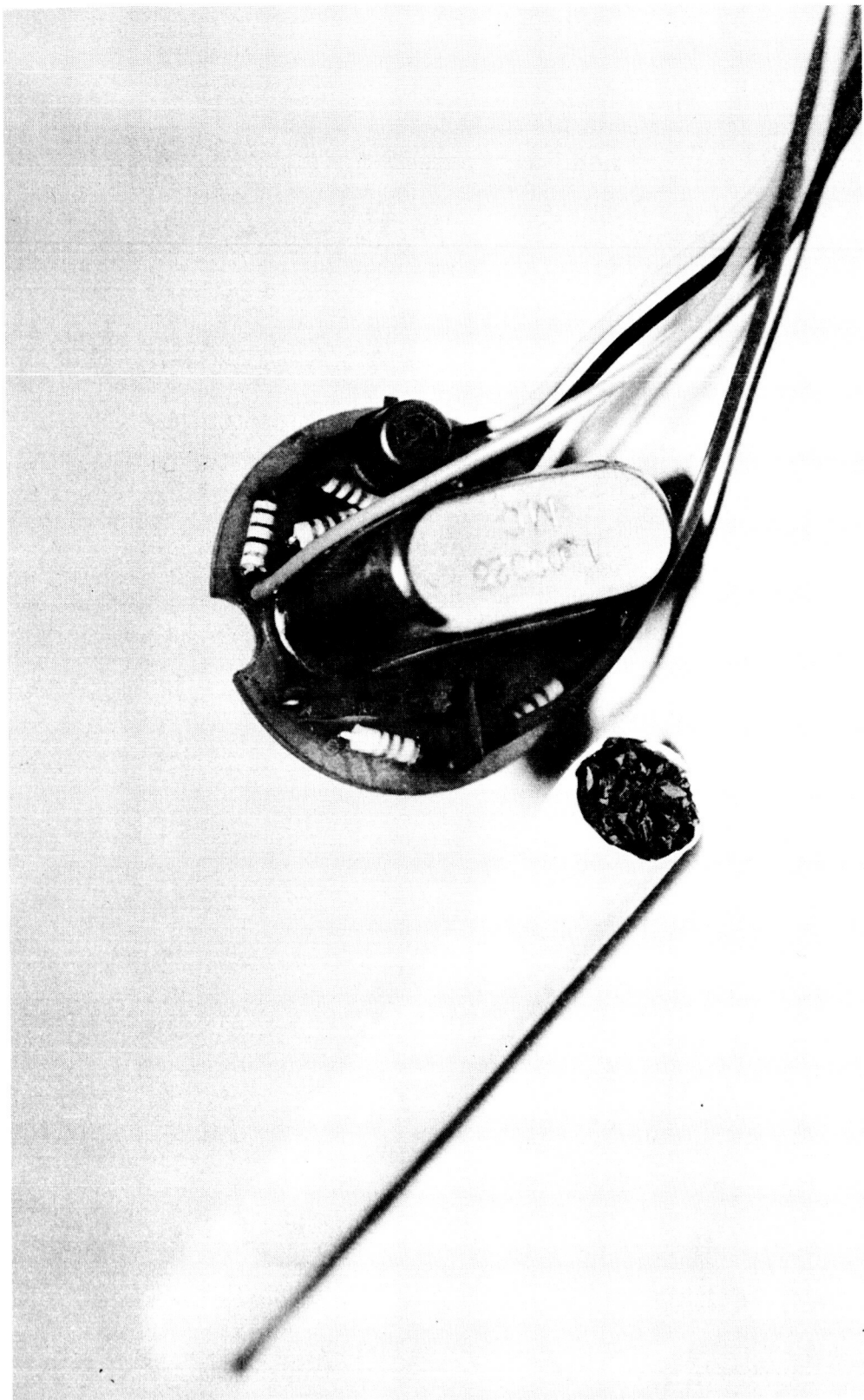
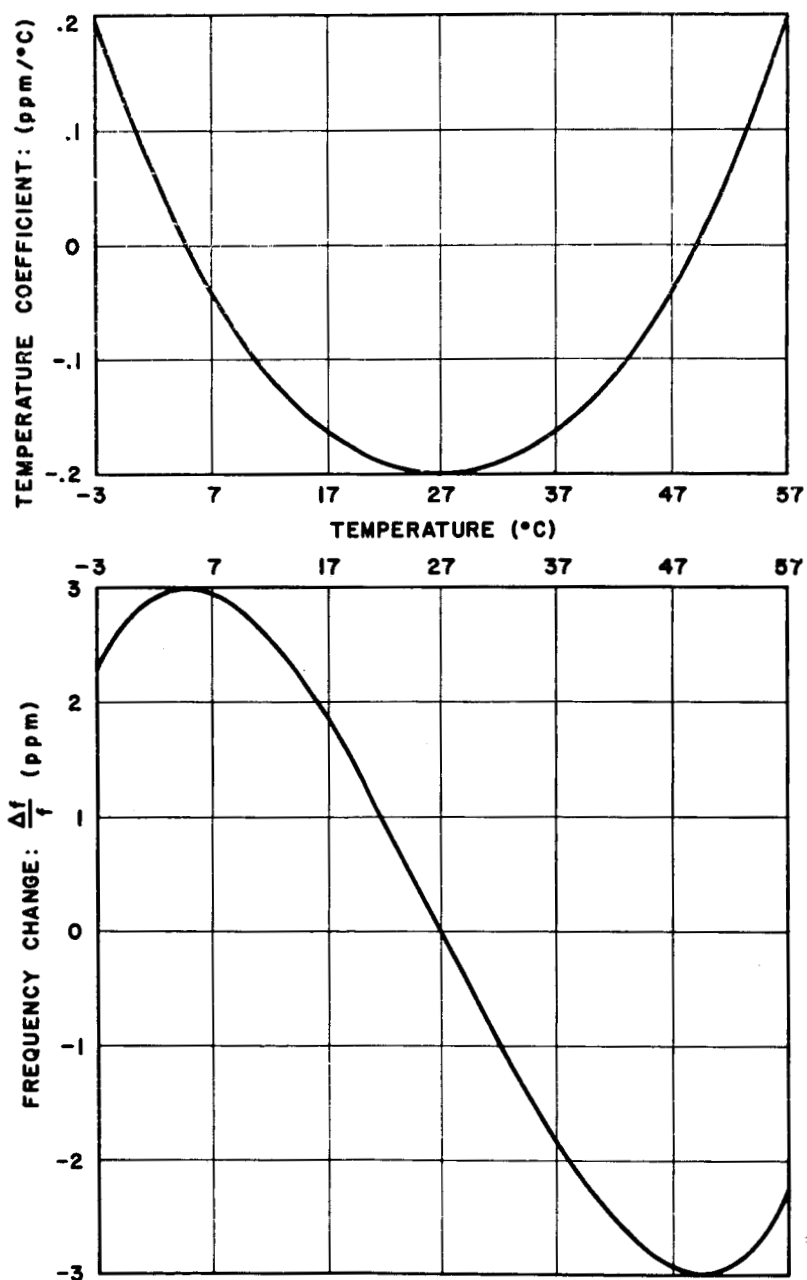Payload S45 AM-19F

Fig. 12

FIG. 13   OSCILLATOR

FIG. 14 TYPICAL OSCILLATOR TEMPERATURE CHARACTERISTICS

temperature change per orbit at the crystal is about $\pm 5°C$ x 4 x 10^{-3}x 10^{-1} or $\pm$ .002°C. Since the maximum temperature coefficient of the crystal is about .20 x 10^{-6} parts per °C (Figure 14), the frequency change per orbit (120 minutes) due to temperature change is about $\pm$ .0004 parts in 10^6 or 4 parts in 10^{10}. Unfortunately, this extreme stability does not exist because of other factors such as circuit noise and voltage variations.

An antiresonant crystal is used so that no inductance is required in the circuit. This allows the oscillator to be as small as possible. The circuit is basically a Colpitts type oscillator with the crystal supplying motional inductance to the circuit and C3 and C4 providing unity feed-back. C3 and C4 are equal, but individually selected to put each crystal on frequency at 27°C. The combination of R1, R2, and R3 determine the amount of negative resistance synthesized by the transistor and presented to the crystal. R2 and R3 form a voltage divider so that the load is loosely coupled to the oscillator to prevent frequency pulling by changes in the oscillator's load. R1, R4, and R6 form a conventional bias network for the transistor. R5 is primarily to keep the feedback signal phase such that negative resistance only (no reactance) is synthesized by the transistor. A Fairchild X1040 transistor is used in the circuit for its low noise and stability of characteristics. The thermistor, RT1, is located near the crystal case and is used to telemeter the crystal temperature in the event it is desired to know where the crystal is operating on the temperature coefficient curve while the beacon is in orbit.

2. 1st Harmonic Amplifier

This is a two stage amplifier that is pretty much conventional in circuitry. It contains an 11 volt diode voltage regulator for the 1.00025 mc oscillator (D1). C5, C7, and C14 help prevent higher harmonics present by stray and direct pickup from entering the oscillator, Q2 and Q3. T1 is an untuned ferrite ring transformer for matching and to allow the ground in the input circuit of Q3 to be between emitter and base signal potential. This tends to make Q3 unilateral so that load changes are not reflected back to Q2 and the oscillator. D2 is for temperature compensation of the gain of Q3.

3. 20 and 27th Harmonic Generator

This circuit employs the capacity diode, D3, in a zero bias, hole storage mode of operation to generate a sharp pulse at the 1st harmonic repetition rate. Q4 clips and amplifies this pulse rich in high order harmonics. The output of Q4 drives the two hybrid crystal filters which are made with balanced windings on the ferrite rings of T2 and T3. C17 and C18 are adjusted to balance out the static

capacity of each crystal so that only the 20th harmonic may pass the top
filter and only the 27th harmonic may pass the lower filter. These
filters must reject signals spaced 1 mc away. Therefore, they have
relatively wide pass bands for crystals so that temperature-frequency
changes in the crystals will not effect the output powers. L6 performs
the function of setting the relationship between 20th and 27th harmonic
power outputs.

4. 20 and 27th Harmonic Limiters

These stages limit signal changes by saturation and build
the 20th harmonic power from 0.1 mw to 8 mw and the 27th harmonic from
0.1 mw to 1 mw. The input circuits are similar to that of Q3 for
unilateral operation and D4, D5, and RT3 compensate the biases of Q5
and Q6 to give constant output as temperature changes. R15 and R19 are
gain controls to set the drive for the next stages. C25 and C31
resonate the outputs and T6 and T7 match the outputs to a 50 ohm load.

5. Phase Modulator and 27th Harmonic Amplifier

The capacity of the capacity diode D6 and the combined
series inductance of L9 and T12 form a series resonant circuit at the
27th harmonic. A backward bias of 9 volts plus an a.c. signal of 4
volts peak to peak at 730 cps are applied to the diode. The 730 cps
swing modulates the diode's capacity and therefore the phase shift in
the series resonant circuit to phase modulate the drive to Q8 by $\pm$ 14°.
This incidentally causes about 6% amplitude modulation at 1460 cps to
the drive of Q8; but since Q8 operates partially saturated, it reduces
the incidental A.M. to less than 6%. The 730 cps is supplied through
the package plug "P" from a subcarrier oscillator in another instrumen-
tation deck. It is frequency modulated with the information to be
telemetered from the satellite. R25 is a gain control to set the
swing on D6 to 4 volts peak to peak. Q8 amplifies the 27th, phase
modulated, harmonic from 1 mw to 45 mw with an efficiency of 53% and a
dissipation of 41 mw. This heat is conducted to the canister by an
electrically insulated heat sink.

6. 108th Harmonic Generator

This circuit uses a capacity diode (D14) to multiply the
signal frequency and angle modulation by four so that its output is 20
mw at the 108th harmonic and modulated $\pm$ 56° (nearly one radian). This
circuit consumes no d.c. power and quadruples frequency with only a
3.5 db loss. Besides input and output frequency resonant circuits, it
contains an idling circuit (C88 and L34) resonant at twice the input
frequency. The design of this type circuit is described in detail in
ABMA Report No. DG-TR-1-59, dated 19 January 1959, "Capacity Diode
Parametric Performance and Circuit Design by a Finite Current Method",
by Alan J. Fisher. A copy of this report may be found in Appendix I.

7. 20th Harmonic Amplifier

This amplifier receives 8 mw of drive and delivers three outputs, 60 mw, 30 mw, and 110 mw. It has a gain of 14 db and an efficiency of 61%. The output is coupled from midway between the emitter and base to make the stage unilateral and to allow electrical and thermal connection of the transistor's case (collector) to the beacon canister for removal of the 125 mw of dissipated power. The 60 mw output (upper output in Figure 11) drives a load whose impedance is modulated at the 1st harmonic rate. To prevent this from amplitude modulating the other two outputs, the three loads are presented to the transistor in series by the use of the ferrite transformers T9, T10, and T11. These are driven through Y4, a fundamental mode crystal series resonant at the 20th harmonic. It allows only current at the 20th harmonic to flow through the three loads, thus eliminating any 1 mc side bands due to the modulated load. The three transformers also match all three outputs to 50 ohms.

8. 40 and 41st Harmonic Generator

This circuit receives 60 mw of power at the 20th harmonic and 3.1 mw at the 1st harmonic. Capacity diode D11 operates in the hole storage mode to double the 20th and to the 40th harmonic. This 40th harmonic energy is partly coupled out of the circuit through the hybrid ferrite ring transformer T13 and the crystal Y5. Part of the 40th energy remains in the diode and is mixed with the 1st harmonic energy to produce the sum, or 41st harmonic. This harmonic is coupled out through T13 and crystal Y6. C54 and C55 balance the static capacities of each crystal so that only energy at the series resonant frequency of each crystal may pass. R32 adjusts the amount of 1st harmonic voltage on the diode and therefore may be used to set the balance between 40 and 41st energy out of the circuit.

9. 40 and 41st Harmonic Power Amplifier

This module consists of two separate transistor amplifiers operating at different frequencies into a common load and load matching circuit. Crystal filters are used to decouple the output of each stage from the other so that the RF voltage swing on each transistor is a simple sine wave allowing maximum efficiency as class "C" amplifiers. The inductance across each crystal is adjusted to be antiresonant with the crystal capacity and C64 and C65 at the frequency of the other stage. Therefore, at the terminals of each crystal there is a reactance zero at the operating frequency of that stage and a reactance pole at the frequency of the opposite stage. The frequencies are only 2.5% apart so that the resonant matching circuit (L22 and C68-69) transforms the signals essentially alike. Each transistor operates with an

efficiency of about 61%, a gain of 12 db, and a dissipation of 70 mw.
To remove the dissipated heat in the vacuum of space, aluminum brackets
are clamped to the transistors and to the beacon canister. This
incidentally grounds the transistor collectors and causes the emitters
and bases (drive terminals) to be above ground by the RF output
potential. This requires the use of an isolation transformer to
drive each transistor. It should be noted that the outputs are taken
midway between bases and emitters to cause the amplifiers to be
unilateral.

10. 20th Harmonic Power Amplifier

This module follows the same design as the 40 and 41st
power amplifier except no crystal filter is required. The stage
efficiency is 70%, gain of 12 db, and the dissipation of 220 mw is
conducted to the beacon canister.

11. 120th Harmonic Generator

This circuit receives 110 mw at the 20th harmonic and
capacity diodes multiply it by six to develop 28 mw at the 120th
harmonic. This circuit has a signal power loss of only 5.9 db. Besides
input and output frequency tuned circuits, it has idler circuits at
twice (C47 and L12) and three times (C48 and L13) the input frequency.
D15 is an 11 volt zener diode for bias control on the two capacity
diodes, D7 and D8. Two diodes were used in parallel simply because no
single diode was readily available with sufficient energy storage and
high enough cutoff frequency. The design technique of this type of
circuit is also described in the Appendix.

12. 120th Harmonic Power Amplifier

This board provides an output of 320 mw at the 120th
harmonic to drive the 360th harmonic generator. The efficiency is 47%,
gain of 10 db and dissipation of 360 mw. This heat is conducted to the
canister by an aluminum bracket which incidentally grounds the collector
of the transistor and causes the drive terminals of the transistor to
be above ground by the RF output potential. Therefore, an isolation
transformer (T14) is necessary to couple the drive to the transistor.
This transformer consists of a number of turns of subminiature coaxial
cable wound on a ferrite ring. Only the coaxial drive currents can
flow unimpeded in the coaxial cable since they have no coupling into
the ferrite. If any of the transistor output current tends to flow
through the cable and return through ground to the collector, it is
impeded or choked by the high permeability ferrite ring. The output
of the transistor is taken midway between emitter and base to cause the
stage to be unilateral. The transistor operates with a d.c. short
between emitter and base so that class "C" operation results from the
emitter junction contact potential.

13. 360th Harmonic Generator

This circuit uses a capacity diode to double to the 240th harmonic and to triple to the 360th harmonic. The design of this type of circuit is also described in the Appendix. The doubling loss in this circuit is only 2.2 db (100 to 60 mw) and the tripling loss is 3.4 db (220 to 100 mw) with no d.c. power consumed.

14. 960th Harmonic Generator

This circuit uses a capacity diode to quadruple frequency to the 960th harmonic and is much like the 108th harmonic generator with an idler (C86 and L31) at twice the input frequency. The design and theory of this type of circuit is also described in the Appendix. The output resonant and matching circuit is composed of a 1/5 wavelength, 100-ohm characteristic impedance, transmission line. This line is printed on the circuit board of 1/8 inch Rexolite with a ground plane for the line printed on the opposite side. C87 is also printed on the circuit board to form a small capacity with reproducible capacitance and stray inductance. This arrangement makes it most inconvenient to tune the distributed resonant circuit at the 960th harmonic. For this reason R35 was employed to adjust the capacity diode bias and thereby tune the 960th harmonic circuit electronically. That is, changing the diode's bias will change the diode's capacity which enters into the resonance of the distributed 960th harmonic circuit.

15. Bias Regulation

These zener diodes supply a fixed bias to several of the capacity diodes in the beacon as may be seen in the wiring diagram of Figure 11.

D. Special Difficulties

1. The metal plating on the thermal capsule cannot have a low inductance connection between it and the canister because this would thermally short circuit the vacuum gap. The rear of all of the circuit boards are in close proximity with this plating on the capsule. Because of this, the plating provided unwanted mutual coupling between several of the circuit boards, particularly between the highest frequency and highest power boards and the 1 mc oscillator located within the capsule. This caused numerous difficulties that were very hard to isolate one from another. For example, at one point it was indicated that the 40 and 41st harmonics were getting onto the leads between the oscillator and 1st amplifier and beating together either in Q1 or Q2 to form a difference frequency of 1.00025 mc capable of driving Q1 without benefit of the oscillator. Also, there was evidence

that a feed back loop at the 20th harmonic existed which involved the thermal capsule plating, and a similar loop seemed to exist at the 27th harmonic. None of these signal loops usually had enough gain to break into active self oscillation, but rather would cause phase jitter at particular supply voltages and temperatures as phase shifts changed. Problems of this general description were solved by some changes in component layout to keep high impedance points away from the rear of the printed circuit boards, particularly in the 20 and 27th harmonic generator and limiters. Aluminum brackets similar to the transistor heat sinks were added to the 1st amplifier, 20th, 27th, 108th, 120th, 360th, and 960th harmonic generators to give them a low inductance ground to the canister, and the wires between the oscillator and the 1st harmonic amplifier were shielded. Also C5 and C7 were added to by-pass any high order harmonics at the termination of these wires.

2. Phase jitter occurred when the 20th harmonic amplifier was driving the 120th harmonic generator, and also when the 27th harmonic amplifier was driving the 108th harmonic generator. The first problem was solved by adding R22, R23, and C34 to the circuit and by putting the three outputs of the 20th harmonic amplifier in series instead of in parallel, as originally designed. The second problem was solved by operating the input to Q8 near ground potential by using an electrically insulated heat sink instead of trying to ground the collector. In both cases it is felt that the cure caused better unilateralization of the amplifiers so that the possibility of approaching self-oscillating conditions, with the extreme range of load impedances possible in an harmonic generator, was reduced.

3. Under certain tuning conditions, phase instability occurs in the 40 and 41st harmonic section of the beacon. This effect has been minimized by diode selection but no way has been found to completely eliminate this under all conditions of tuning. However, after each beacon is tuned, it is subjected to the full range of supply voltages and temperatures simultaneously to assure that instability will not occur. Also during other environmental tests this output is closely watched to see that no such difficulty occurs.

4. During testing of the environmental model of the beacon, it was discovered that the 20th harmonic was being unintentionally phase modulated by telemetry at about .02 radian. Because of the frequency multiplication, this caused the 40 and 41st harmonics to be .04 radian, 360th to be .36 radian, and 960th to be .96 radian. This effect was traced to less than perfect unilateralization of the 27th limiter so that the reactance modulation occurring in its output load is slightly coupled backwards into the 20 and 27th harmonic generator, the common origin of both signals. No cure, short of a redesign of the whole 27th and 108th harmonic section, could be found. The only disadvantage of this effect is that the 960th carrier power is

reduced by about 2 db because of the loss of energy to the side bands. The effect may be an advantage in that it provides redundancy for telemetering in the event the 108th harmonic failed and also it may simplify signal identification. Therefore, no redesign was made.

III. GENERAL OPERATING PROCEDURE

Before operating the equipment, the following checks should be made:

1. All five R.F. outputs of the beacon should be connected by a 50 ohm shielded line to a dummy load or antenna whose impedance is approximately 50 ohms resistance at the respective output frequencies. These output terminals are arranged by descending frequency from the top (lid end) of the beacon canister to the bottom. Thus the top coaxial connector is 960th harmonic output, the next is the 360th, the middle is 108th, the next to bottom is 40 and 41st, and the bottom is 20th harmonic output (see Figure 10).

2. The 1 mc test signal line, pins "k" and "a" of the beacon test socket at the bottom of the wiring channel, should be connected by a 50 ohm shielded line to a 50 ohm load (shield to pin "a").

3. The cables which connect to pin "j" of the test socket and pins "d" and "e" of the package plug should not have any d.c. conductance between any of them and common ground in the payload, before they are connected to the beacon package. Pin letters appear on the insulator body of both the package plug and test socket.

4. The beacon package test socket should have pin "b" connected to pins "c", "d", "e", "f", and "h", either by shorting leads or through ammeters.

After these checks have been made, a supply voltage ranging from 14.4 volts to 18 volts may be applied to the beacon package plug by connecting the positive line to pins "b" and "c" and the negative line to pin "a". This is the only power source required for operating the beacon. The power to pin "c" may be keyed for the purpose of keying all R.F. outputs of the beacon including the 1 mc test signal. When the supply voltage is connected to the beacon it should be operating with the following nominal characteristics at 15.6 volts and room temperature.

```
20th harmonic output power -------------400 mw
40 and 41st harmonic output power-------200 mw
108th harmonic output power------------ 20 mw, angle modulated
                                          one radian
```

```
                360th harmonic output power-------------100 mw -0.3 db/cable
                                                                foot
                960th harmonic output power------------ 10 mw -1.0 db/cable
                                                                foot
                Total continuous current, plug pin "b"--140 ma
                Keyed current, plug pin "c"------------- 4 ma
                Modulation signal, plug pin "d" to "e"-- 9 volts peak to peak
                20 harmonic P.A. current, socket pin "c" 38 ma
                40 and 41st harmonic P.A. current,
                    socket pin "d"---------------------- 22 ma
                27th harmonic amplifier current, socket
                    pin "e"---------------------------- 5.5 ma
                120th harmonic P.A. current, socket
                    pin "f"---------------------------- 43 ma
                20th harmonic amplifier current, socket
                    pin "h"---------------------------- 21 ma
                Modulator test signal, socket pin "j"--- 4 volts peak to peak
                                                         and 9 volts d.c.
                1 mc test signal, socket pin "k"-------- 2 volts peak to peak
                                                         across 50 ohms
```

If any of the above indications are in error by more than 10%, the data booklet for the particular unit under test should be referred to since it provides characteristics at various temperatures and supply voltages for each unit. The serial number of each set is indicated by RMA color code in the wiring channel (Figure 10). If more than a 10% error exists between this data and actual operation, personnel from M-G&C-IR should be notified.

IV. TESTING AND RESULTS

A. Outputs vs Temperature and Voltage

The five radio frequency outputs were monitored while the beacon was operating in a temperature chamber. Temperature and supply voltage were varied to obtain the results. The temperature range was selected on the basis of the discussion in part II, C, 1., of this report and the fact that thermo balance test of the satellite indicated that less than this temperature range could be maintained. The supply voltage range was determined at the lower limit by degradation of beacon output powers and at the upper limit by avoiding any danger of transistor voltage breakdown. Also a practical voltage range had to be allowed for the satellite storage battery and solar cell system to operate efficiently. Thus the voltage range was set at 14.4 to 18 volts and the temperature range at -3 to +57°C. Typical results of this test are shown in Figure 15. The most likely beacon temperature in orbit is about 20°C with an occasional rise up to 40°C for a few days. Since only the sum of the 40 and 41st harmonic energy
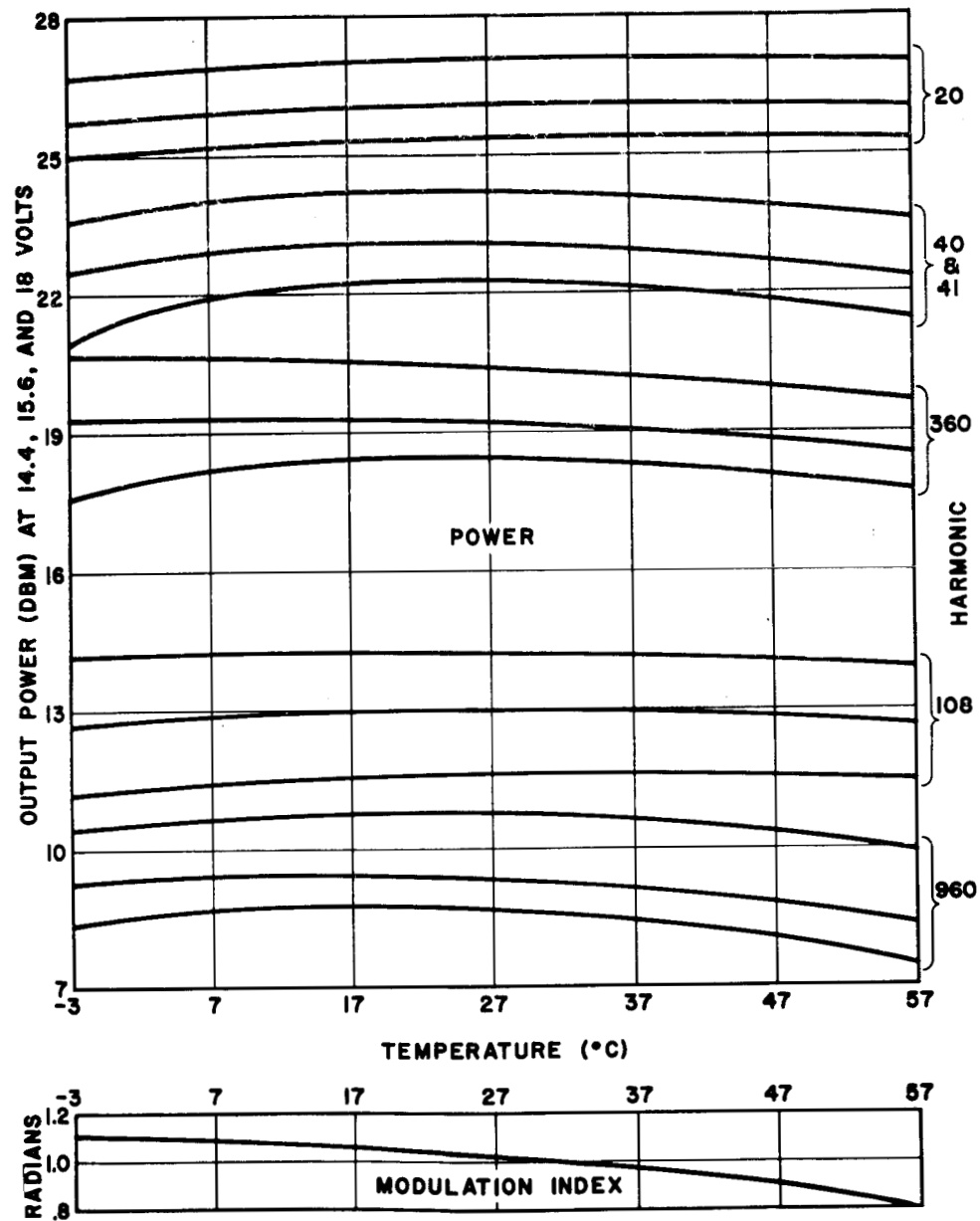
FIG. 15 TYPICAL POWERS AND MODULATION INDEX VERSUS TEMPERATURE

is measured, an indication of their relative powers is of interest. This may be obtained by displaying the signal on an oscilloscope or by detecting it so that the ratio of minimum to maximum signal envelope voltage across a 50 ohm load may be determined. With this information and with the value of total signal power as measured by an rms power meter, the individual 40 and 41st powers may be determined. The nomograph of Figure 16 has been constructed to simplify this calculation. The difference between the 40 and 41st harmonic output powers was generally less than 2 db over the temperature and voltage range. The exact data is presented in data booklets for each transmitter. These booklets are available from M-G&C-IR, Redstone Arsenal, Huntsville, Alabama.

B. Frequency Stability

The frequency stability is determined by crystal temperature, supply voltage, and circuit noise, in that order of importance. The crystal temperature and supply voltage are telemetered from the satellite. Therefore, their effects can be corrected, if required. The first basic test of stability was made with temperature and supply voltage held as constant as possible to determine the limit of stability possible. This was done at room temperature and a National Company Atomichron with a stability of at least 1.5 parts in 10^{10} was used as a frequency standard in the test. This test indicated the limiting stability of the beacon frequencies to be 1.3 parts in 10^9 for time periods of 30 minutes or longer. Next the supply voltage was varied to determine its effect on frequency. Using a beacon supply voltage of 15.6 volts as reference, the frequencies increased by 9.4 parts in 10^8 at 18 volts and decreased by 5.0 parts in 10^8 at 14.4 volts. These changes are caused partly by some of the energy from the beacon's outputs affecting the oscillator because with these outputs turned off, the corresponding frequency changes are only 2.5 and 3.1 parts in 10^8. The frequency changes caused by temperature may be estimated by the use of the telemetered temperatures along with Figures 6, 8 and 14. In general, this will be less than one part in 10^8 but may become nearly one part in 10^7 under the relatively rare conditions which may occur just before and just after the satellite experiences 100% sunlight for a few days.

C. Modulation Index

During test "A", the modulation index of the 108th harmonic output was monitored and the result was plotted in the lower part of Figure 15. The effect of supply voltage changes is too small to be shown. For this test, a 730 cps, 9 volt, peak to peak signal was applied between pins "d" and "e" of the package plug and R25 was adjusted to provide 4 volts peak to peak at pin "j" of the beacon test
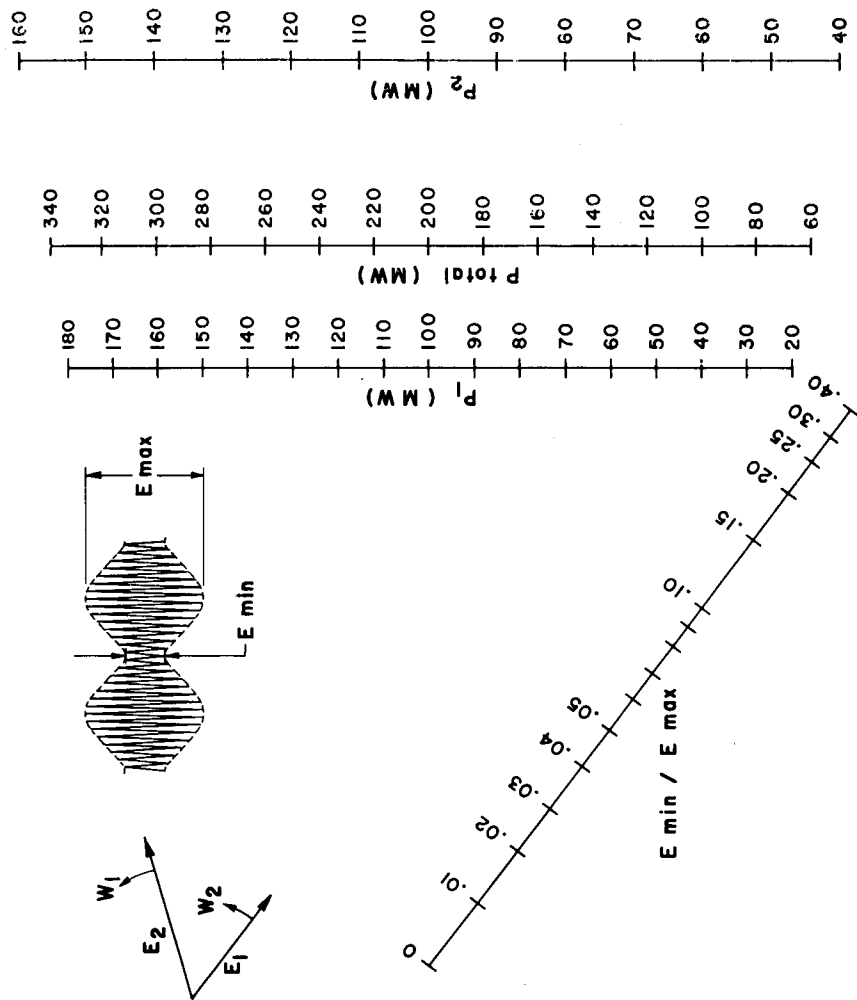
36

FIG. 16 POWER DIVISION NOMOGRAPH

socket. The modulation index was noted on a frequency deviation meter and then the modulation signal source was increased to 10Kc and adjusted for 4 volts again at pin "j". The modulation index was again read to be the same to check linearity. The test was then run with the 10Kc signal to obtain a more accurate reading of small changes in the index.

D. Vacuum Soak Test

The beacon was operated for five days in a vacuum chamber at pressures below 5×10^{-4}mm of mercury. During this time the temperature was changed about every 12 hours alternately from 15 to 50°C. Temperatures below 15°C could not be obtained at the beacon without cooling the skin of the payload excessively. Results of this test showed that all outputs degradated by 1 to 1.5 db below the values obtained in the test of part "A". This degradation occurred gradually as the test proceeded. This effect is probably caused by outgasing and further curing of the ruggedizing compound on the circuit boards since all outputs could be returned to normal after the test by slight retuning of the beacon.

E. Spin Test

The beacon was operated through slip rings on a centrifuge with the spin axis coaxial with the cylindrical shape of the canister. A spin rate of 420 rpm was obtained and the output powers and 1st harmonic frequency were measured. No change due to spin could be found.

F. Vibration Test

The beacon was operated on a vibration machine and subjected to random noise vibration (20 to 2000 cps) for two minutes at 20 g rms in the direction of rocket thrust. Then it was similarly vibrated for 2 minutes each at 13 g rms in the two axis mutually perpendicular to the direction of rocket thrust. The only effect of vibration found was some noise modulation in the outputs. However, the 108th harmonic output was received by a typical ground station receiver during this test and telemetry was recorded with no difficulty. After the test the beacon operated just as it did before. In a previous test with blank circuit boards, an accelerometer was mounted on some of the boards and it was determined that a mechanical amplification of only 1.2 existed on these boards.

G. Shock Test

The beacon while inoperative was subjected to thirty 25 g impulses which attained the g level in approximately 90 milliseconds.

The acceleration was in the direction of rocket thrust. The beacon operated exactly the same after the test as it had before.

H. **Miscellaneous**

1. Weight

a. Complete Beacon Deck: 11.4 pounds

b. Thermal Capsule: 7.1 pounds

2. Size

The overall size of the beacon deck is 5.606" in height by 7.500" in diameter.

V. PROJECT BY-PRODUCTS

A. **Extrapolated Harmonic Generator Performance**

By organizing the performance of the numerous capacity diode harmonic generators designed for this equipment, it should be possible to extrapolate and predict the more general capabilities of this type of circuit. Such data should be very useful for the design of future systems. This was done by using the theoretical loss vs the normalized frequency curve for doublers as developed in the report of the Appendix and shown in Figure 13 of that report. The characteristics of the frequency doubling in the 360th harmonic generator and those of another laboratory developed doubler were plotted on this graph. Since the curve represented diode losses only, it needed to be displaced downward by $\frac{1}{2}$db to agree with the two experimental points plotted. This indicated a loss of $\frac{1}{2}$db in the tuned circuits in addition to the diode loss. Points were plotted for the other harmonic generators in the beacon and these suggested the group of curves shown in Figure 17. The two points on the x2 curve are the laboratory developed doubler and the doubling from 120 to 240 mc in the 360th harmonic generator. The point on the x3 curve is the tripling from 120 to 360 mc in the 360 mc harmonic generator with a 3.5 db loss. The points on the x4 curve are the quadrupling from 27 to 108 mc in the 108th harmonic generator with a 3.45 db loss; and the quadrupling in the 960th harmonic generator with a loss of 6.4 db. The point on the x6 curve is for the 120th harmonic generator multiplying 20 to 120 mc with a 5.8 db loss. The curves are drawn with an unnormalized frequency scale which assumes diodes with a cutoff frequency (where Q=1) of 15Kmc at four volts bias. This value is typical of state of the art devices today. Because some of the diodes used had slightly different cutoff frequencies, the points are proportionally offset on the frequency scale. Also plotted

EXTRAPOLATED HARMONIC
GENERATOR PERFORMANCE

Fig. 17
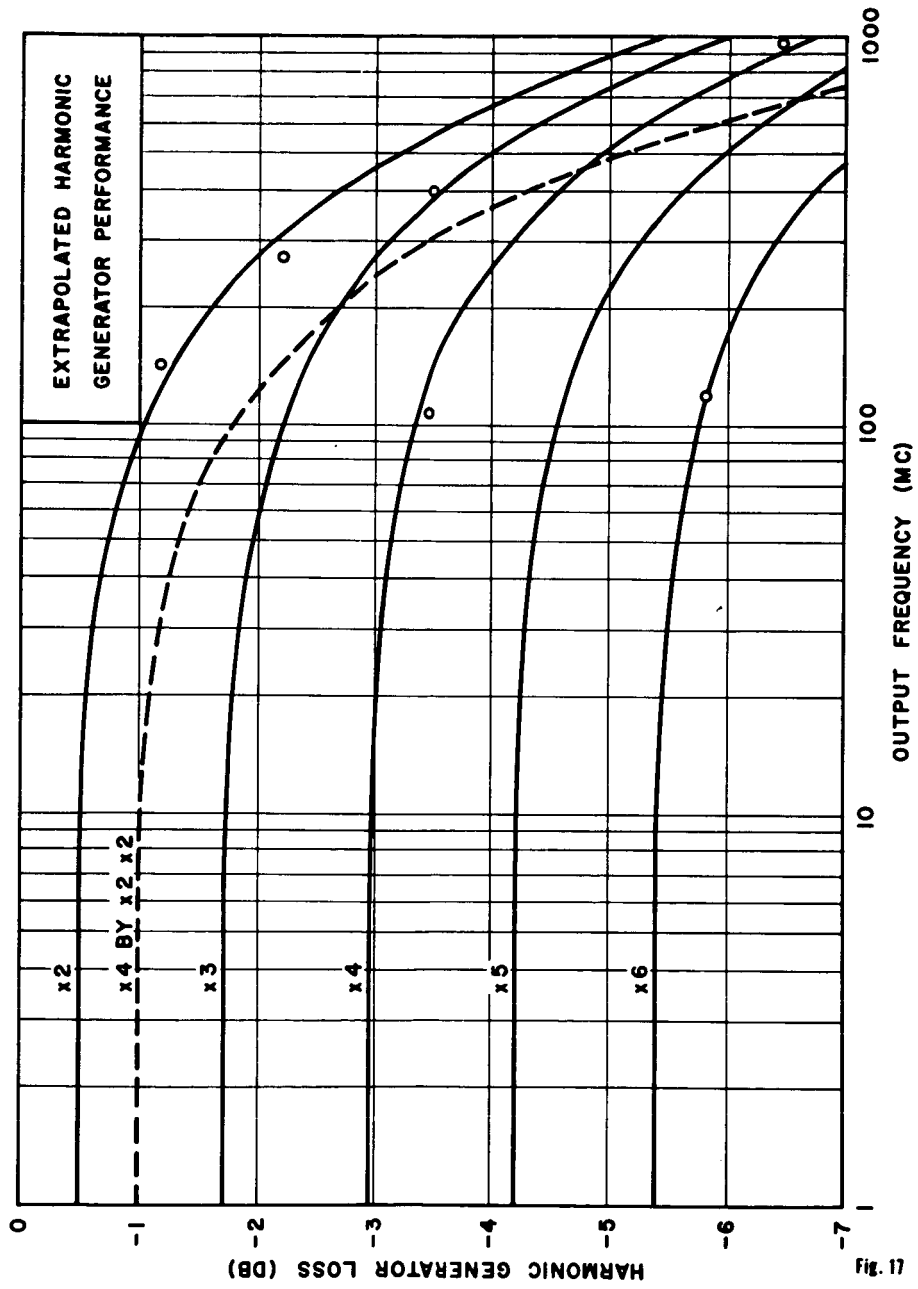
by the dashed curve is quadrupling by the use of two diodes in cascaded doublers and this curve shows that quadrupling is done more efficiently by this method at frequencies below about 460 mc output frequency. A similar situation can be shown to exist in the x8 case.

B. Other Applications for the Thermal Null Filter

The technique developed for the thermal null filter probably has numerous other applications in manned and unmanned satellites or even in long term weather measurements by filtering out periodic temperature variations. The design need not be a sphere or cylinder. It could equally well be panels of low diffusivity material shunted with occasional metal rods and surfaced with metal foil. The panels could be used to surround living quarters or instrument space. The thickness of the panel would be proportional to the square root of the material's diffusivity and inversely proportional to the square root of the null frequency. Because of the one-half power relation, very slow periodic changes could be filtered out with surprisingly thin panels.

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APPENDIX

ABMA REPORT NO. DG-TR-1-59

CAPACITY DIODE PARAMETRIC PERFORMANCE
AND CIRCUIT DESIGN
BY A FINITE CURRENTS METHOD

DEVELOPMENT OPERATIONS DIVISION

CAPACITY DIODE PARAMETRIC PERFORMANCE AND CIRCUIT DESIGN

BY A FINITE CURRENTS METHOD

by

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ABSTRACT.

If a finite number of sinusoidal currents rather than voltages are
permitted to exist in a capacity diode parametric device, the perform-
ance will be more efficient and more easily calculated. A two-current
analysis of frequency doubling (and halving) is presented which shows
the relationships between efficiency and power and diode cutoff frequency.
Input and output coupling circuits which approximate the two-current
analysis are shown. The analytic results are used to predict the gener-
ation of watts of efficient microwave power by all solid state devices.
Finally, the extension of the finite currents method to higher harmonics
and parametric mixers, amplifiers and oscillators is discussed.

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LIST OF ILLUSTRATIONS

TABLE OF SYMBOLS

c_b — small signal capacity at breakdown voltage $\left.\dfrac{dq}{de}\right]_{e=E_b}$

c — small signal capacity at any reverse voltage; $\dfrac{dq}{de}$

c_0 — linear component of junction capacity at a bias of E_0

E — junction voltage

E_0 — dc component of junction voltage; bias

E_d — voltage at diode terminals

E_b — reverse breakdown voltage of the diode

e — instantaneous diode junction voltage (reverse)

e' — component of e which results from the nonlinearity of junction capacity and charge

$e'_{2\omega}$ — component of e' at the subscript angular frequency

F — ratio of peak ac charge to peak fundamental component of ac charge

f — lowest frequency of diode current

f_b — diode cutoff frequency; frequency at which diode small signal reactance near breakdown voltage equals diode resistance

I_ω — peak amplitude of lowest frequency diode current

i — diode current

$i_{2\omega}$ — diode current at the subscript frequency

K — defined by equation (22)

m — ratio of peak fundamental to peak second harmonic diode current

n — any number; a frequency ratio

η — ratio of second harmonic power leaving to fundamental power entering the diode terminals; diode doubling efficiency

v

η_c power efficiency of circuits coupling diode to driving generator and load

P power

P' power handled in the lossless junction

$P'_{2\omega}$ power entering or leaving the lossless junction at the subscript frequency

Q_b charge stored in the junction just before breakdown; $(2c_b E_b)$

Q junction charge

Q_o dc component of junction charge

q ac component of junction charge

$\hat{q}$ peak ac component of junction charge

R_G matched driving generator resistance

R_L matched load resistance

R'_ω resistance encountered by fundamental current due to e'

$R'_{2\omega}$ resistance encountered by second harmonic current due to e'

r diode series resistance

t time

ω lowest angular frequency of diode current

ω_b angular frequency at which diode small signal reactance near breakdown voltage equals diode resistance

SECTION I. INTRODUCTION

The analytic methods of this article are applicable to harmonic and subharmonic generators, parametric mixers, amplifiers, and oscillators which employ the capacity diode. An analysis is needed so that the circuit designer may predict the impedance, power level and efficiency of these capacity diode devices, and so that the diode designer may know what characteristics are desirable. Usually when an analysis is attempted, circuitry is assumed which allows only a finite number of sinusoidal voltages to exist across the diode. This results in several infinite series which describe the complex current that flows. If, instead, circuitry is assumed which allows only a finite number of sinusoidal currents to flow through the diode, simple mathematics suffice to describe the performance of the devices. At most frequencies the only dissipative (and noisy) element of a capacity diode is a series resistance. Therefore, least power is lost if only those currents are allowed to flow which are necessary to the function required of the diode. Thus, for the reasons of best efficiency and simplest calculations, the finite currents method is advantageous. In order to demonstrate the simplicity of the method it is first necessary to develop an equivalent circuit for a model diode (Section II) and then examine the applicability of the equivalent circuit to actual diode types (Section III).

SECTION II. DERIVATION OF A CAPACITY DIODE EQUIVALENT CIRCUIT

The capacity of a classical abrupt diode junction is proportional to the junction voltage to the minus one-half power. This relationship allows a simple equivalent circuit to be developed. It will be shown in another section that graded junctions, which follow a one-third power law, may be assumed to follow this one-half power law over a voltage range of 100:1 if another element is added to the equivalent circuit to be developed here. Therefore, this derivation may be applied to almost any type of capacity diode ranging from an abrupt to a graded junction.

The object here is to derive the diode voltage in the form of a sum of voltage terms which will each describe a series element in an equivalent circuit. An abrupt junction is assumed here so that:

$$\frac{c}{c_b} = \sqrt{\frac{E_b}{E}} \; ; \tag{1}$$

where c is the variational junction capacity at the reverse junction voltage E and c_b is the variational junction capacity measured at some convenient voltage, E_b, for a particular diode. Since the breakdown voltage of the diode will be of interest later, it is convenient to make E_b the breakdown voltage and c_b the variational junction capacity at (or near) breakdown. The variational capacitance of (1) may be rearranged:

1

$$\frac{dQ}{dE} = c = c_b \sqrt{\frac{E_b}{E}} \quad ; \tag{2}$$

and by integrating, the junction charge is:

$$Q = 2c_b \sqrt{E_b E} \tag{3}$$

and by rearranging:

$$E = \frac{(Q)^2}{4(c_b)^2 E_b} \tag{4}$$

For the junction voltage, E, to always be a reverse voltage in the presence of a signal, it must contain a dc or bias component E_o. This results in a steady component of junction charge Q_o which may be determined from (3):

$$Q_o = 2c_b \sqrt{E_b E_o} \tag{5}$$

The ac charge may now be obtained by subtracting the steady component from the total charge:

$$q = Q - Q_o \quad \text{or} \quad Q = Q_o + q \tag{6}$$

and by substituting (5) for Q_o:

$$Q = 2c_b \sqrt{E_b E_o} + q \tag{7}$$

and substituting (7) into (4):

$$E = \frac{(2c_b \sqrt{E_b E_o} + q)^2}{4(c_b)^2 E_b} = \frac{4(c_b)^2 E_b E_o + 4q c_b \sqrt{E_b E_o} + (q)^2}{4(c_b)^2 E_b} \tag{8}$$

$$E = E_o + \frac{q}{c_b \sqrt{\frac{E_b}{E_o}}} + \frac{(q)^2}{4(c_b)^2 E_b} \tag{9}$$

but from (2) the junction capacity at the bias voltage is:

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$$C\Big]_{E=E_o} = c_o = c_b \sqrt{\frac{E_b}{E_o}} \qquad (10)$$

Therefore the junction voltage is:

$$E = E_o + \frac{q}{c_o} + \frac{(q)^2}{4(c_b)^2 E_b} \qquad (11)$$

Usually the junction reactance is small compared to the parallel junction back resistance so that the latter is negligible. If this is the case, the diode may be thought of as simply the reactive junction in series with the diode spreading resistance r. Then the total voltage at the diode terminals is:

$$E_d = \frac{dq}{dt} r + E_o + \frac{q}{c_o} + \frac{(q)^2}{4(c_b)^2 E_b} \qquad (12)$$

and this may be represented by the equivalent circuit of Fig. 1-a where e' is the voltage generated from the nonlinear component of junction capacity. Note that for circuit design a change in bias voltage, E_o, affects only the linear capacity and not the e' generator.

Figure 1-b shows graphically the half parabola of equation (4). This parabola may be broken down into the sum of the two dashed voltage components; the slope of the linear one corresponds to the c_o of the equivalent circuit and the parabolic one corresponds to the e' generator. As E_o is changed the linear (tangent) component of Fig. 1-b changes and the non-linear component remains the same parabola but displaced.

SECTION III.   CORRECTIONS FOR NONABRUPT JUNCTIONS, SHUNT CAPACITY AND
            BARRIER POTENTIAL

The variational capacity vs voltage of a diode junction may be meas-ured with a small signal impedance bridge and the series resistance component, r, may be measured at the same time if the measuring frequency is high enough. The breakdown voltage should be determined first in a circuit which limits the breakdown current to nondestructive value so that breakdown voltage is not exceeded in the bridge measurements. A plot of the capacity vs voltage should then be made on log-log scales. The slope of the plotted curve will be greatest at mid-voltages and less at low and high voltages. This is due to barrier potential providing a minimum bias and therefore limiting the maximum capacity, and at high voltages the minimum capacity may be limited by the fixed shunt capacity

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$$i = \frac{dq}{dt} \qquad r \qquad c_o = c_b \sqrt{\frac{E_b}{E_o}} \qquad e'$$

$$\longleftarrow ir \longrightarrow \qquad E_o + \frac{q}{c_o} \qquad \frac{(q)^2}{4(c_b)^2 E_b}$$

$$\longleftarrow E \longrightarrow$$

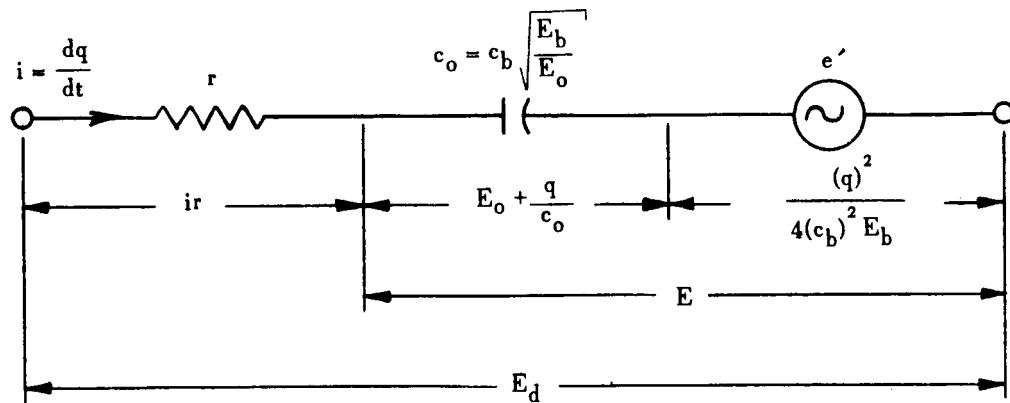$$\longleftarrow E_d \longrightarrow$$

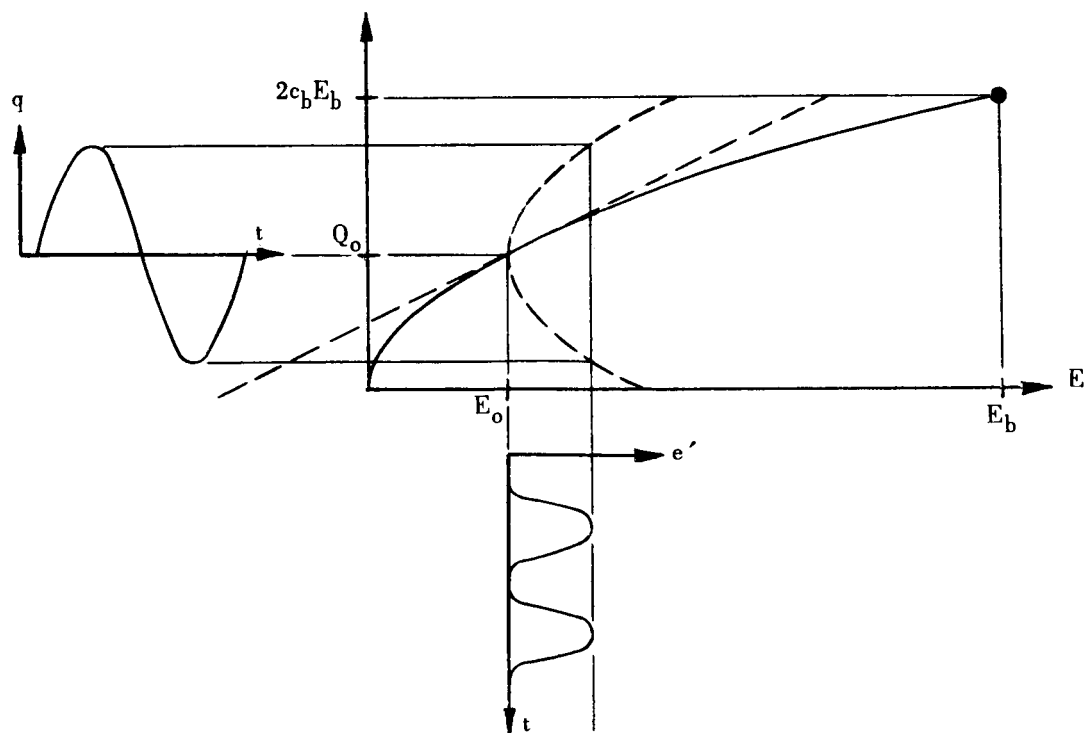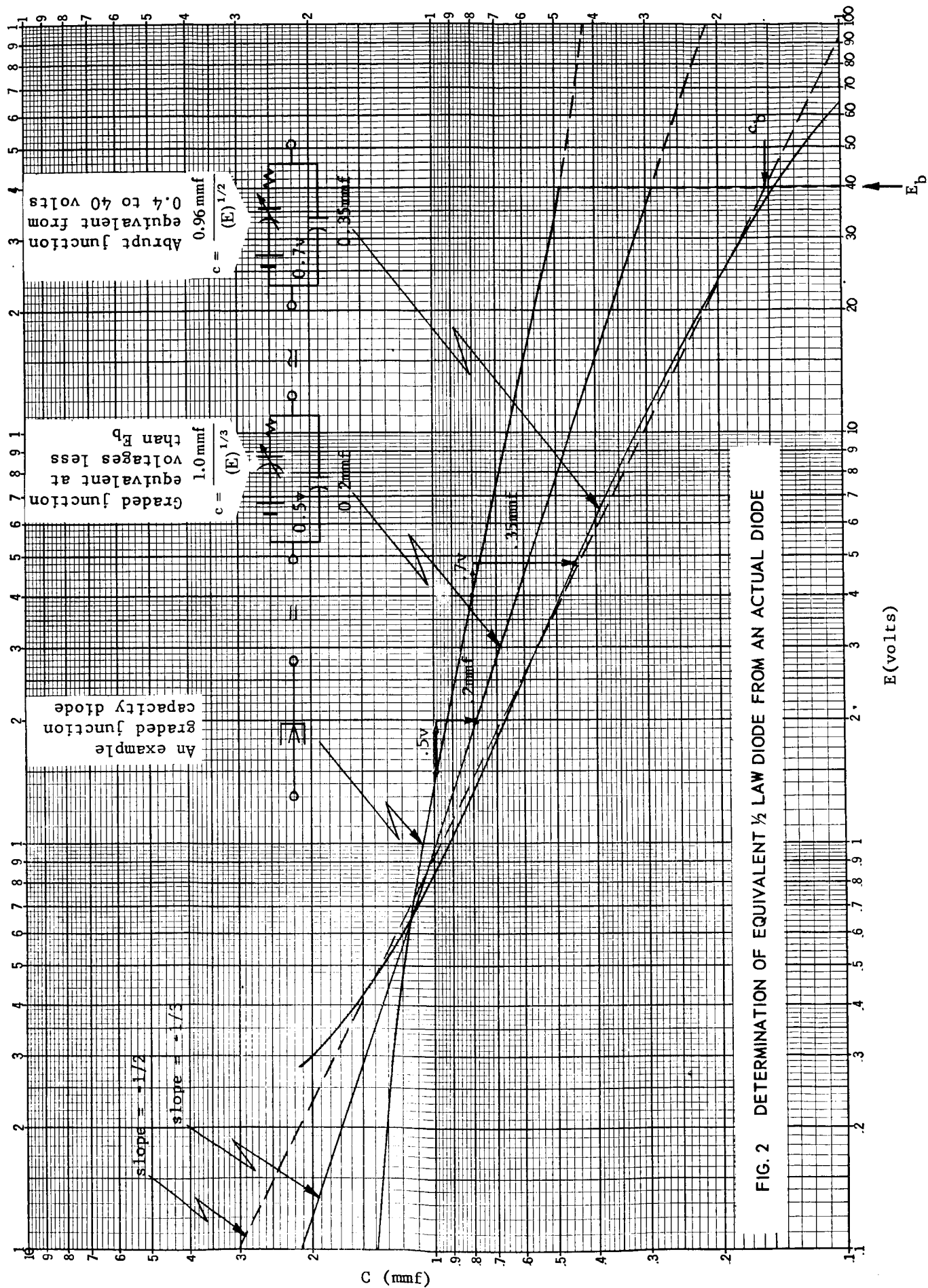FIG. 1-a.   CAPACITY DIODE EQUIVALENT CIRCUIT

FIG. 1-b.   THE PARABOLIC RELATIONS OF JUNCTION CHARGE AND VOLTAGE

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of the diode mount, etc. These effects must be removed from the curve so that a value of c_b to be used in the equivalent circuit may be determined. This may be done by adding the barrier potential to each experimental point plotted and by subtracting the shunt capacity from each point. The correction voltage will be a few tenths of a volt and the holder capacity may be estimated. By trial and error the exact voltage and capacity corrections should be determined which cause the corrected curve to have a straight line negative slope of one to two decades (minus one-half power). If the diode has an abrupt junction it will be possible to choose corrections which result in a corrected curve that exactly fits this straight line relationship. If the diode has a graded junction, it may be made to exactly fit a straight line with a slope of minus one-third. However, since the equivalent circuit assumes an abrupt junction, corrections should be made which cause the corrected curve to fit most closely a straight line with a slope of minus one-half. Figure 2 shows an example of this correction. The curve with least slope is a plot of variational capacity vs voltage for example graded junction diode (-1/3 power). By trial and error it may be determined that by correcting with 0.5 volt and 0.2 mmf the resulting curve will be a straight line with minus one-third slope as shown. Also by trial and error it was determined that if 0.7 volt is added to and 0.35 mmf subtracted from all points of the original curve, the resulting curve fits a straight line with the desired slope of minus one-half for two decades of voltage. Therefore, the example graded junction diode may be represented as a minus one-half power diode (from 0.4 to 40 volts) with a fixed shunt capacity of 0.35 mmf, a barrier potential of 0.7 volts, and a c_b of .153 mmf as shown in the figure. Therefore, the equivalent circuit developed for an abrupt junction may be used for this graded junction if a shunt capacity of 0.35 mmf is added to it. Frequently this shunt capacity is small compared to the c_o of the equivalent circuit and can be neglected. If it is not negligible, it admittedly causes difficulty in establishing a finite current circuit, but the finite current approach will still provide approximate performance and circuit design data. The idealized abrupt junction is not usually found in practice. Practical diodes have capacity and voltage related by negative exponents ranging between 1/2 and 1/3. For this reason the intermediate graphical step in Figure 2 is only of academic interest. In practice one should try to immediately find the corrections which lead to a plot most nearly approximating a minus one-half slope straight line so that the corrected c_b to be used in the abrupt junction equivalent circuit may be obtained as shown in the figure. The barrier potential is of no consequence in the equivalent circuit since it may be included in the E_o value assumed in Section II.

SECTION IV. THE FINITE CURRENTS METHOD

The equivalent circuit developed in the preceding section directly suggests the finite currents method of operation and analysis. If the diode is to be used as a parametric device, current at a number of

C (mmf)

An example graded junction capacity diode

Graded junction equivalent at voltages less than E_b

$$c = \frac{1.0\,mmf}{(E)^{1/3}}$$

Abrupt junction equivalent from 0.4 to 40 volts

$$c = \frac{0.96\,mmf}{(E)^{1/2}}$$

slope = -1/2

slope = -1/3

.5v

.7v

0.2mmf

0.35mmf

.2mmf

.35mmf

c_b

E_b

E(volts)

FIG. 2   DETERMINATION OF EQUIVALENT ½ LAW DIODE FROM AN ACTUAL DIODE

frequencies will have to flow through the diode and a number of voltages will have to exist across the diode junction. If the circuits connected to the diode allow only those voltages necessary to the required function to exist across the diode, many currents will flow at unnecessary harmonic and sum and difference frequencies. These unnecessary currents dissipate power by flowing through r and so cause extra signal power loss in the circuit. In addition it is most difficult to calculate the ac current or charge from the equivalent circuit from a known diode voltage. This suggests the use of a parallel component equivalent circuit, but both a nonlinear reactance and conductance are necessary for this so that exact calculations are still most discouraging. However, if the circuits connected to the diode allow only those currents necessary to the required function to flow through the diode, minimum power loss is achieved and the calculations are simple. The following section shows this simplicity by deriving the frequency doubling efficiency from the equivalent circuit developed and assuming the finite currents type of circuit.

1. Frequency Doubling

a. Derivation of Efficiency and Impedances. For maximum efficiency only those currents necessary to doubling should be allowed to flow through the diode (through r). Therefore, assume the circuit connected to the diode allows only the fundamental and second harmonic currents to flow. Therefore let:

$$\frac{dq}{dt} = i = I_\omega \cos \omega t + m\, I_\omega \cos 2\omega t; \qquad (13)$$

where I_ω is the peak amplitude of fundamental current and m is the ratio of peak second harmonic current to peak fundamental current and the phase angle is assumed.

Then by integrating:

$$q = \frac{I_\omega}{\omega} \sin \omega t + \frac{m I_\omega}{2\omega} \sin 2\omega t \qquad (14)$$

so that from the equivalent circuit:

$$e' = \frac{(q)^2}{4(c_b)^2 E_b} = \frac{\left(\frac{I_\omega}{\omega} \sin \omega t\right)^2 + \frac{m(I_\omega)^2}{\omega^2} \sin \omega t\, \sin 2\omega t + \left(\frac{m I_\omega}{2\omega} \sin 2\omega t\right)^2}{4(c_b)^2 E_b} \qquad (15)$$

The squaring of the charge produces voltage components at ω, 2ω, 3ω, and

4ω as well as dc voltages. For the purpose of calculating input and output power of the junction, only the ω and 2ω voltage components are of interest since current flows only at these frequencies. These voltages from (15) are:

$$e'_\omega = \frac{+m(I_\omega)^2}{8E_b(\omega c_b)^2} \cos \omega t; \quad e'_{2\omega} = \frac{-(I_\omega)^2}{8E_b(\omega c_b)^2} \cos 2\omega t \qquad (16)$$

and the average powers entering and leaving the junction is one-half the product of each peak current and voltage, so from (13) and (16):

$$P'_\omega = \frac{+m(I_\omega)^3}{16E_b(\omega c_b)^2} \quad ; \quad P'_{2\omega} = \frac{-m(I_\omega)^3}{16E_b(\omega c_b)^2} \qquad (17)$$

Since the signs indicate fundamental power entering the junction and second harmonic power leaving, the phase angle assumed in (13) is valid for a doubler. The powers are of course equal because a reactance cannot dissipate power and r has not as yet been considered. The power handled by the junction is either P' of (17). Therefore, the net output power from the diode terminals is $P'-(mI_\omega)^2 r$ and the total input power to the diode is $P'+(I_\omega)^2 r$ so the efficiency is:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P' - (mI_\omega)^2 r}{P' + (I_\omega)^2 r} = \frac{1 - \dfrac{(mI_\omega)^2 r}{P'}}{1 + \dfrac{(I_\omega)^2 r}{P'}} \qquad (18)$$

Instead of operating with r it is convenient to define a diode cutoff frequency in terms of r. Let this be the frequency at which the diode small signal reactance at breakdown voltage is equal to r. Therefore, this cutoff frequency is:

$$\omega_b = \frac{1}{rc_b} \qquad (19)$$

and substituting (19) into (18):

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$$\eta = \frac{1 - \dfrac{(mI_\omega)^2}{P'\omega_b c_b}}{1 + \dfrac{(I_\omega)^2}{P'\omega_b c_b}} ; \qquad (20)$$

and transforming (17):

$$(I_\omega)^2 = \left[\frac{16P'E_b(\omega c_b)^2}{m}\right]^{2/3} ; \qquad (21)$$

and substituting (21) into (20):

$$\eta = \frac{1 - (m)^{4/3}\, K\dfrac{\omega}{\omega_b}}{1 + \left(\dfrac{1}{m}\right)^{2/3} K\dfrac{\omega}{\omega_b}} ; \quad \text{where } K = \left[\frac{256(E_b)^2\omega c_b}{P'}\right]^{1/3} \qquad (22)$$

Solutions to equation (22) are plotted in Figure 3. By examining equation (22) and Figure 3 it may be seen that efficiency increases as P' increases. This trend is limited by avalanche breakdown of the diode at a value of P' which causes the diode peak voltage to exceed E_b and the diode peak charge to exceed $Q_b = 2c_b E_b$ from equation (3). Therefore, the maximum peak to peak value the ac charge may obtain is $2c_b E_b$ because dissipative breakdown and forward conductance bracket the maximum and minimum values of charge possible without excessive power loss (Fig. 1-b). Therefore, the maximum peak amplitude of ac junction charge is:
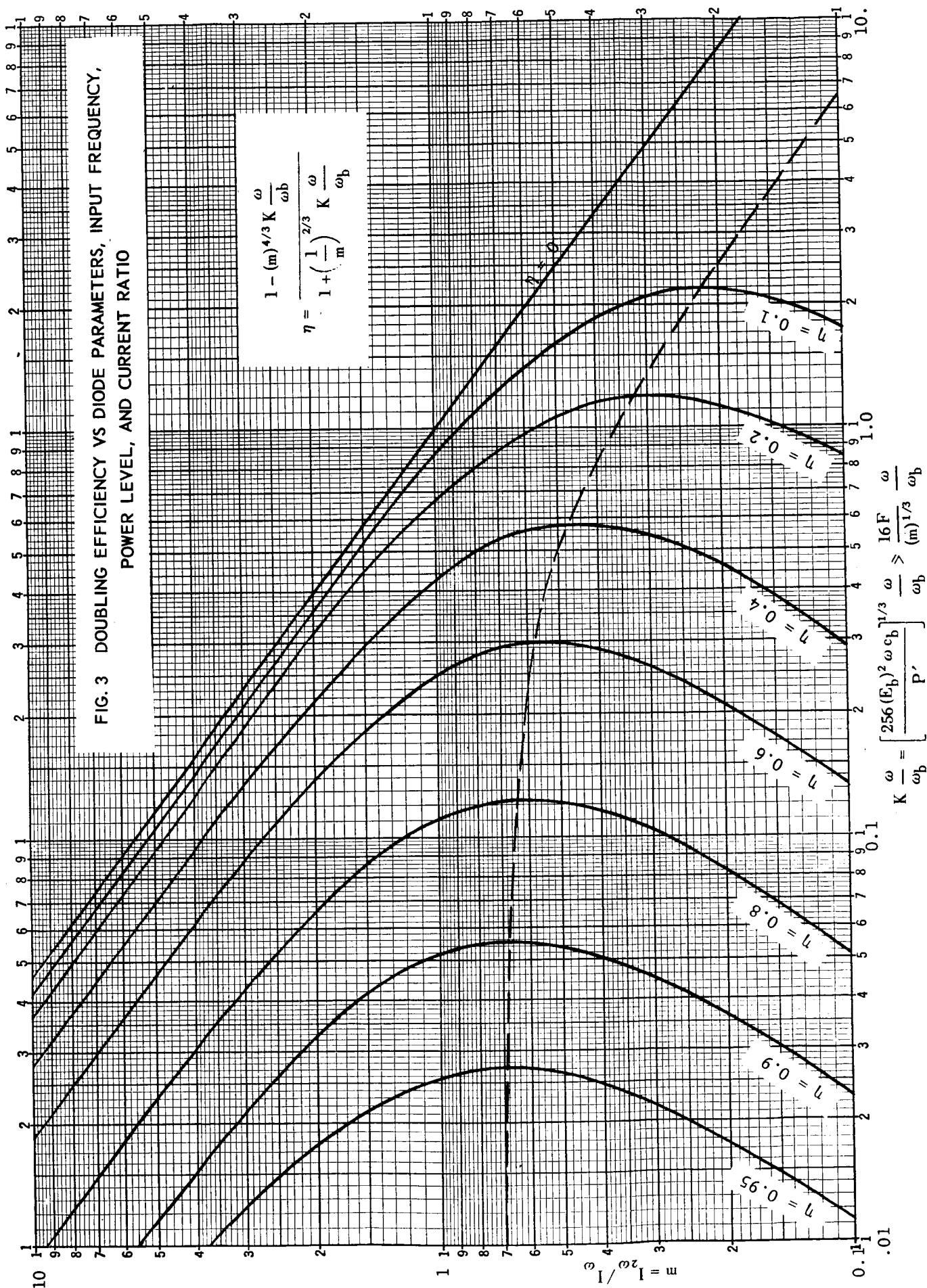
$$\hat{q}\Big]_{max} = c_b E_b \qquad (23)$$

Also the peak values of q may be written from equation (14) as:

$$\hat{q} = F\frac{I_\omega}{\omega} ; \quad \text{where F is the ratio of peak ac} \qquad (24)$$
charge to peak fundamental charge
and is plotted in Fig. 4 as derived
from eq. (14).

Combining (23) and (24):

FIG. 3 DOUBLING EFFICIENCY VS DIODE PARAMETERS, INPUT FREQUENCY, POWER LEVEL, AND CURRENT RATIO

$$\eta = \frac{1 - (m)^{4/3} K \dfrac{\omega}{\omega_b}}{1 + \left(\dfrac{1}{m}\right)^{2/3} K \dfrac{\omega}{\omega_b}}$$

$$K \frac{\omega}{\omega_b} = \left[\frac{256 (E_b)^2 \omega c_b}{P'}\right]^{1/3} \frac{\omega}{\omega_b} \geq \frac{16 F}{(m)^{1/3}} \frac{\omega}{\omega_b}$$

$\eta = 0.1$

$\eta = 0.2$

$\eta = 0.4$

$\eta = 0.6$

$\eta = 0.8$

$\eta = 0.9$

$\eta = 0.95$

$m = I_{2\omega} / I_\omega$

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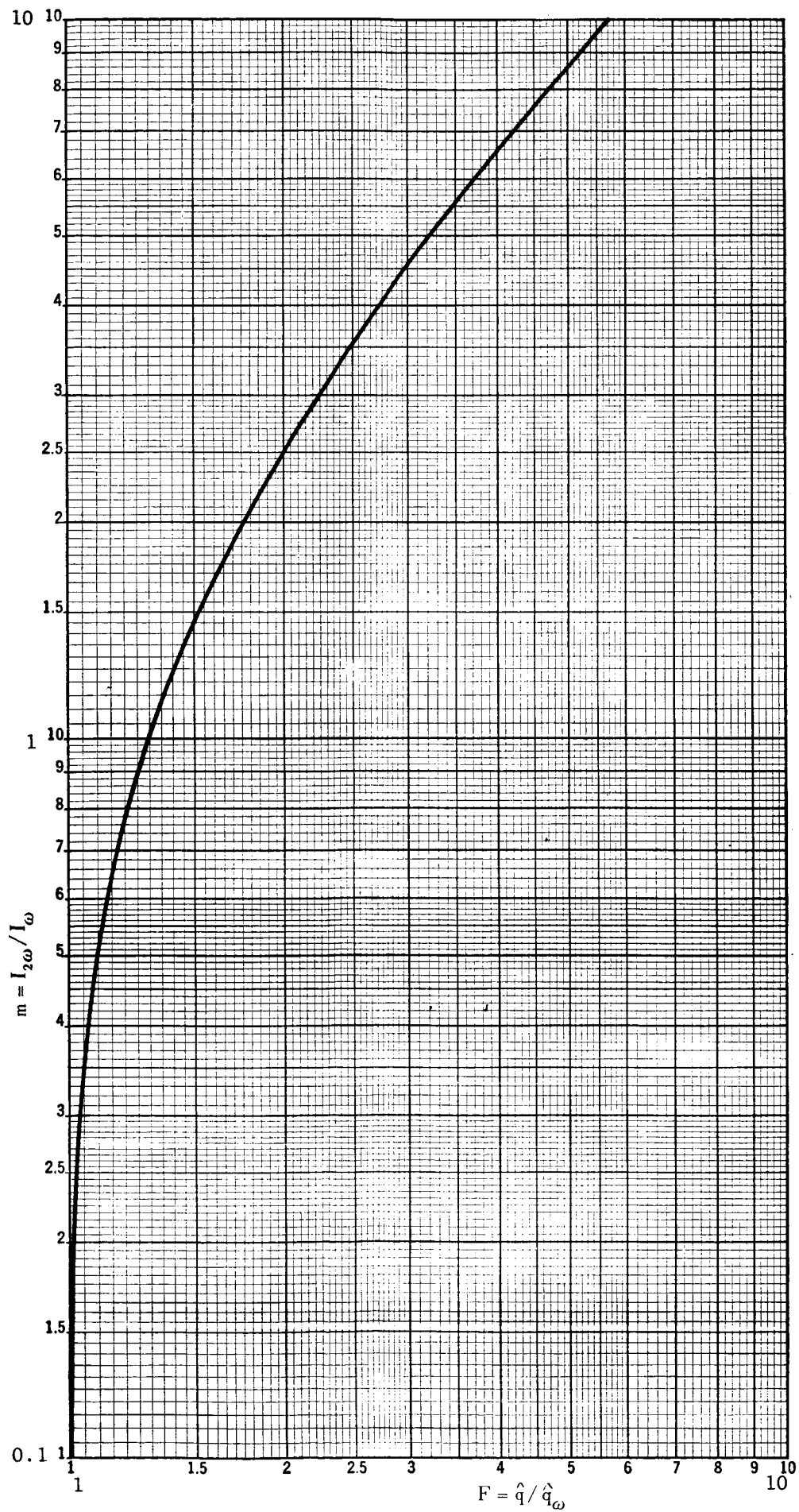
FIG. 4. RELATION OF THE F AND m RATIOS

The vertical axis is labeled $m = I_{2\omega}/I_\omega$ and the horizontal axis is labeled $F = \hat{q}/\hat{q}_\omega$.

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$$I_\omega\big]_{max} = \frac{\omega c_b E_b}{F} \qquad\qquad (25)$$

and from (17) and (25)

$$P'\big]_{max} = \frac{m(E_b)^2 \omega c_b}{16(F)^3} \qquad\qquad (26)$$

and combining (26) and (22); $K\big]_{min} = \frac{16F}{(m)^{1/3}}$ so then from (22):

$$\eta\big]_{P'=max} = \frac{1 - 16mF\frac{\omega}{\omega_b}}{1 + \frac{16F}{m}\frac{\omega}{\omega_b}} \qquad\qquad (27)$$

Solutions to equation (27) are plotted in Figure 5. This figure shows the diode maximum efficiency which occurs at the highest power level allowed by E_b. The efficiency is in terms of the ratio of second harmonic to fundamental diode current and the ratio of input frequency to diode cutoff frequency. If the diode is operated at less than its maximum power, Figure 3 should be consulted to determine the efficiency, but Figure 5 always limits the maximum efficiency of the diode since P' of Figure 3 is limited by equation (26).
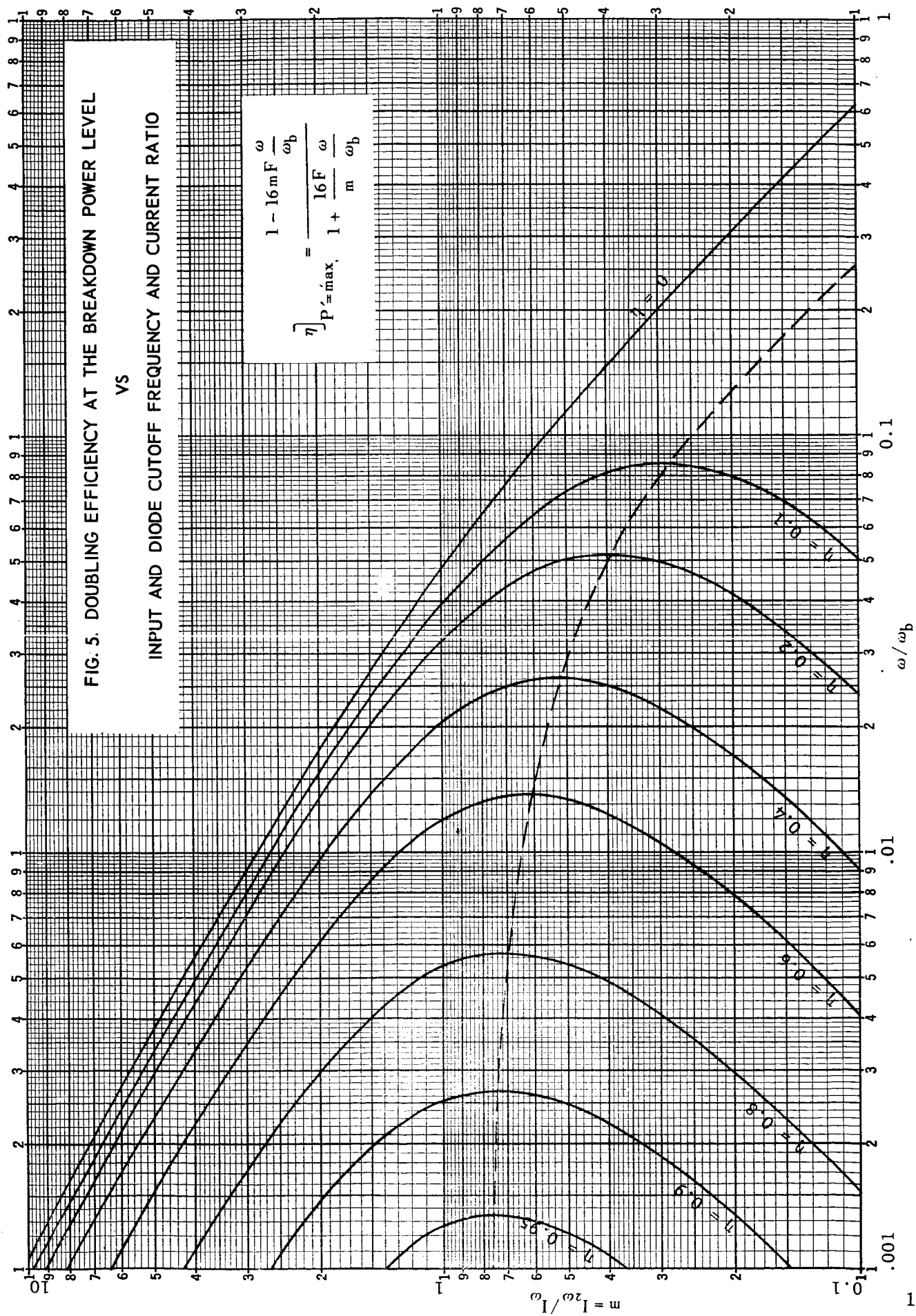
The equivalent resistance encountered by I_ω within the nonlinear reactance may be determined from (13), (16) and (21) to be:

$$R'_\omega = \frac{mI_\omega}{8E_b(\omega c_b)^2} = \left[\frac{(m)^2 P'}{32(E_b)^2(\omega c_b)^4}\right]^{1/3} \qquad\qquad (28)$$

and like an ideal impedance transformer:

$$R'_{2\omega} = \frac{-R'_\omega}{(m)^2} \; ; \; \text{since } P'_\omega = P'_{2\omega}$$

In order to obtain the actual resistances to be matched by circuits external to the diode, the resistance $r = 1/\omega_b c_b$ must be taken into account; so the matched driving generator resistance is:

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FIG. 5. DOUBLING EFFICIENCY AT THE BREAKDOWN POWER LEVEL
vs
INPUT AND DIODE CUTOFF FREQUENCY AND CURRENT RATIO

$$\eta \rfloor_{P' = \text{max}} = \frac{1 - 16\,\text{mF}\,\dfrac{\omega}{\omega_b}}{1 + \dfrac{16F}{m}\,\dfrac{\omega}{\omega_b}}$$

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$$R_G = \left[\frac{(m)^2 P'}{32(E_b)^2 (\omega c_b)^4} \right]^{1/3} + \frac{1}{\omega_b c_b} \tag{30}$$

and the matched load resistance is:

$$R_L = \left[\frac{P'}{2(m)^4 (E_b)^2 (\omega c_b)^4} \right]^{1/3} - \frac{1}{\omega_b c_b} \tag{31}$$

It is well to note that the matched values of R_G and R_L vary with P' so that a constant amplitude signal is preferred. However, the signal frequency may vary a great deal since the reactances and resistances encountered in the device allow great signal band widths.

If the object of the derivation had been to determine frequency halving efficiency, the form would have been nearly the same and the halving results would be the same as Figures 3, 4, and 5 except that the meaning of m in these figures would have been $I_\omega/I_{2\omega}$.

The preceding derivation of efficiency and impedances may be employed to determine the diode required for a particular doubler as shown in the following example:

Let the target performance of the example doubler be:

f_{in} = 100 mc; f_{out} = 200 mc

P' = 0.1 watt

η = 0.9 (so m = 0.7 from Fig. 3 and F = 1.17 from Fig. 4)

R_L = 50.0 ohms

$R_G = (m)^2 R_L$ = 24.5 ohms

It is convenient to determine first the diode which will barely handle the power and then add a safety factor to prevent the possibility of diode breakdown. From equation (3) the charge stored in the junction at or near breakdown is $Q_b = 2c_b E_b$. The energy stored is $Q_b E_b/2 = c_b(E_b)^2$ joules. By rearranging (26) this energy stored may be stated as:

$$c_b (E_b)^2 = \frac{16(F)^3 [P']_{max}}{\omega m} = \frac{16(1.17)^3 \times 0.1}{2\pi \times 10^8 \times 0.7} = 5.82 \times 10^{-9} \text{ joules} \tag{32}$$

This simply means that the required diode must be able to store at least

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this energy just before breakdown occurs. There are infinite sets of E_b and c_b which will satisfy this requirement but the particular set is determined by the R_L chosen. At this high efficiency $r = 1/\omega_b c_b$ must be quite small compared to R_L, so from (31):

$$R_L \simeq \left[\frac{P'}{32(m)^4 (E_b)^2 (\omega c_b)^4}\right]^{1/3} \tag{33}$$

and substituting (26) for P' and rearranging:

$$\left.\frac{1}{\omega c_b}\right]_{P'=max} \simeq 8mFR_L = 8 \times 0.7 \times 1.17 \times 50 \tag{34}$$

$$= 327 \text{ ohms reactance at breakdown at 100 mc}$$

From this c_b may be determined to be 4.87 mmf and from (32) E_b must be 34.6 volts. For the required efficiency, Figure 5 shows that ω/ω_b or f/f_b must be no more than about .0027, so with f=100 mc; $f_b = \frac{100}{.0027} = 37$ K mc (the highest f_b currently reported is 150 K mc).

To sum up the required diode characteristics:

$$f_b = \frac{1}{2\pi r\left[c\right]_{34.6 \text{ volts}}} \gtrless 37 \text{ K mc at 34.6 volts reverse}$$

$$E_b \gtrless 34.6 \text{ volts breakdown}$$

$$\left. c\right]_{34.6 \text{ volts}} = 4.87 \text{ mmf}$$

b. <u>Input and Output Coupling Circuits</u>. The main requirement of these coupling circuits is that they not allow the 3ω and 4ω voltages across the diode, indicated in equation (15), to cause a current to flow at these frequencies. The existance of these voltages across the junction cannot dissipate any power. However, current at these frequencies through r would dissipate unnecessary power and thus would lower the doubling efficiency. The circuit shown in Figure 6 prevents the flow of these currents if the LC ratios are large. However, with practical inductances this means a series resistance from the coils which is probably large compared to the diode r. If LC ratios are chosen which do not spoil efficiency too much, it is then necessary to place a capacity across the driver and an inductance across the load to prevent part of i_ω from flowing through R_L and part of $i_{2\omega}$ from flowing through R_G. It is then necessary to calculate new values of R_G and R_L because of the impedance
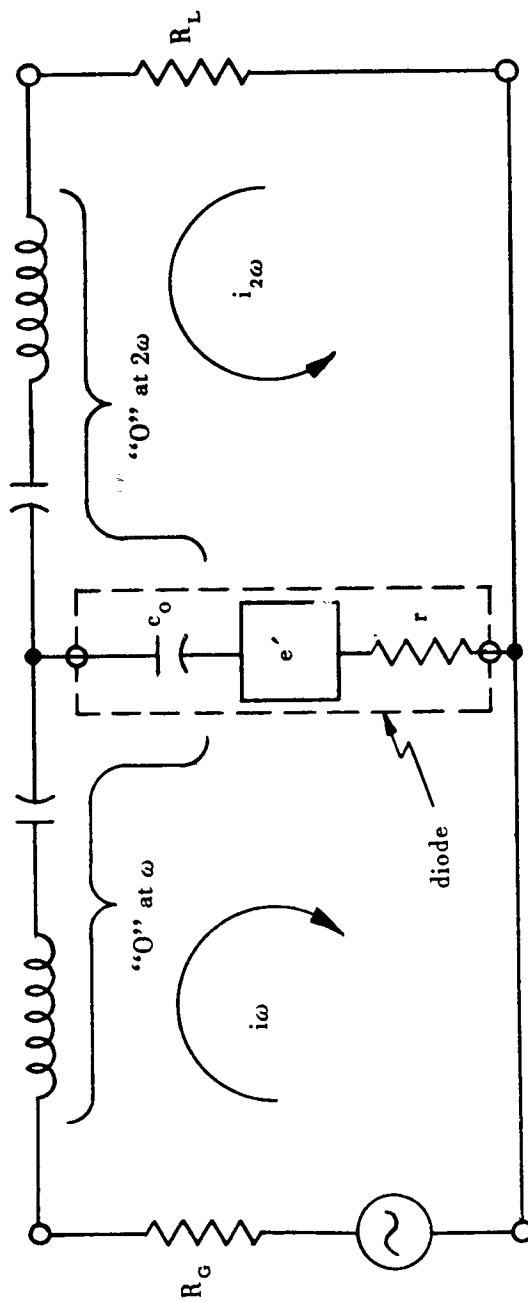
15

FIG. 6.   A FREQUENCY DOUBLING CIRCUIT

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transformation caused by these shunt reactances. Such a circuit has been tried at 50 mc and an efficiency of 78% resulted instead of the calculated 85% doubling efficiency. The extra power loss was in the above described coupling circuit. Another coupling circuit was developed which should reduce the coupling losses. It is shown in Figure 7. This circuit places an inductance in series with the diode which cancels out the linear capacity component of the diode at 1.4ω, the geometric mean of ω and 2ω. Then the diode leg of the circuit looks capacitive at ω and inductive at 2ω. The series leg to the driving generator contains a reactance pole to $i_{2\omega}$ and looks inductive to i_ω. The series leg to the load contains a reactance pole to i_ω and looks capacitive to $i_{2\omega}$. The three LC ratios are chosen so that i_ω and $i_{2\omega}$ each flow in resistive loops and are prevented from flowing in the other loop by the reactance poles. The inductance L in series with the diode presents a large reactance at 3ω and 4ω to discourage diode current flow at these frequencies.

Still another possible arrangement is shown in Figure 8. The coupling circuits are shown as coaxial lines but could be parallel lines, printed strip lines, etc. For ultrahigh frequencies this coupling method is mandatory for good coupling efficiency. It operates as follows: The shorted stub at tee A places an open at the top of tee A for ω and a short for 2ω. This allows ω power to enter the system and prevents 2ω power from leaving the system through tee A. The open stub at tee C places an open at the top of tee C for 2ω and a short for ω. This allows 2ω power to leave the system and prevents ω power from leaving the system through tee C. The shorted stub at tee B is a quarter wave length long at 3.5ω so that at 3ω and 4ω it places a large reactance in series with the diode to discourage the flow of current at these frequencies.

At frequency 2ω a short exists at tee A and since length A-B is a quarter wave length for 2ω, an open appears in the left exit of tee B for 2ω. The right exit of tee B leads directly to a matched 2ω load. This load therefore sees the diode simply in series with the inductance of the series stub. This inductance may be made to cancel the capacitive reactance of the diode at 2ω by choosing the proper Z_0 for the stub. At frequency ω a short exists at tee C so that at the right exit of tee B there appears an inductive reactance equal to the characteristic impedance of the quarter-wave section B-C. The left exit of tee B leads directly to a matched ω generator. This generator therefore sees the diode reactance in series with a small inductive reactance of the central stub and these in parallel with the inductance just described. These three reactances may be made to cancel and transform the input resistance of the diode to match the line.

    c. <u>Bias Considerations</u>. Self-bias has the obvious advantage that no constant voltage bias supply is required. It incidentally causes the minimum charge to be approximately zero. It has the disadvantage
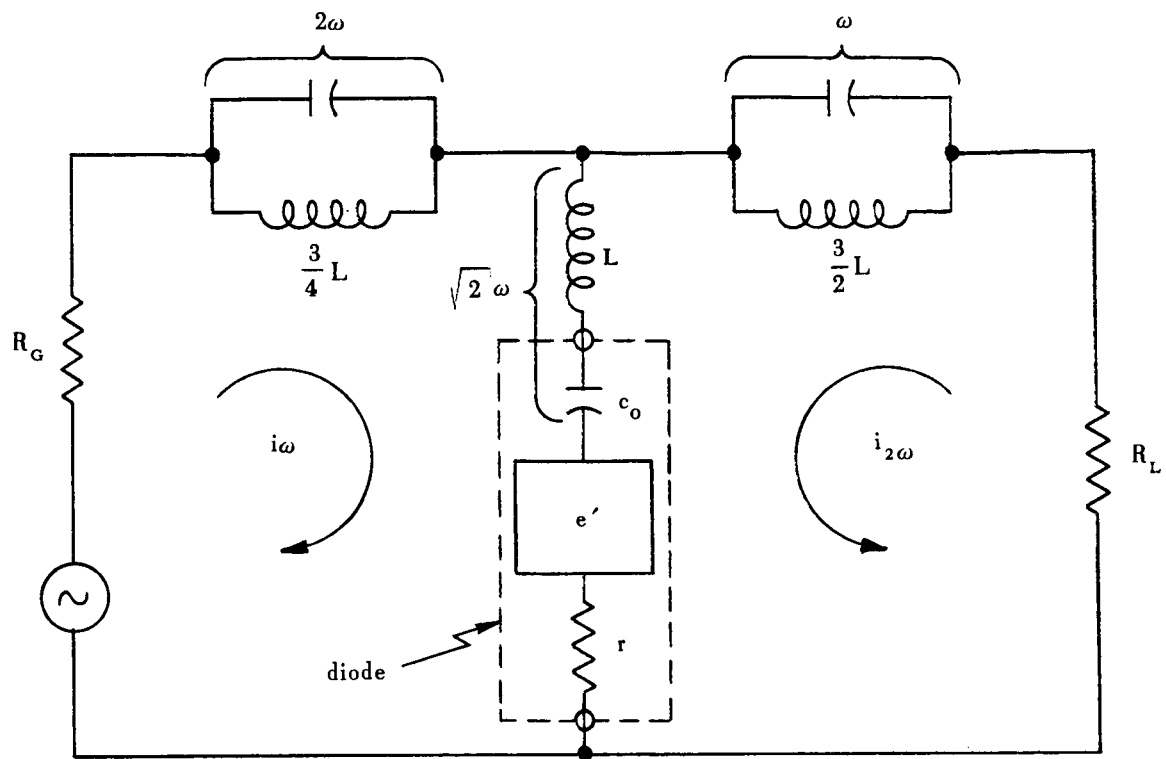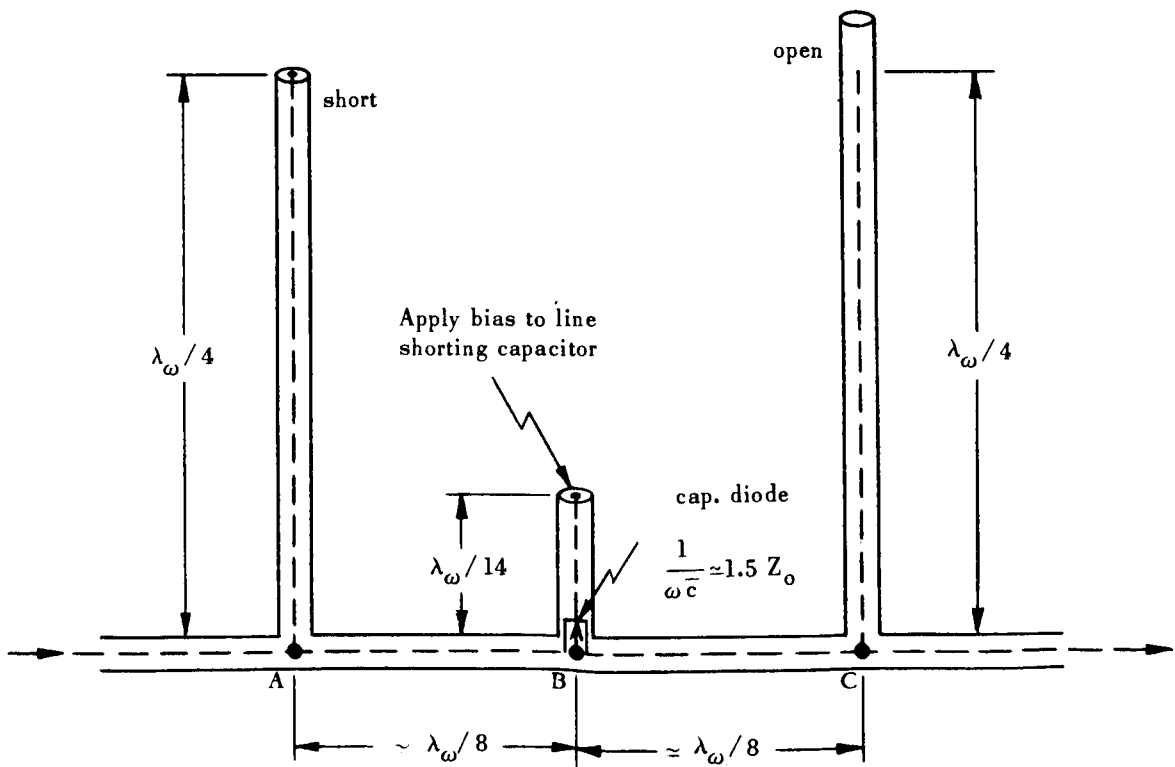
FIG. 7. A FREQUENCY DOUBLING CIRCUIT WITH TRAPS

FIG. 8. A COAXIALLY COUPLED DOUBLER

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that adjustment of the circuit is difficult because as resonance is approached the self-bias will increase, changing the diode reactance, and, therefore, changing the target resonant point of the component being adjusted. This effect causes critical adjustments that may result in practically no doubling if an adjustment is slightly in error. This poses a strong argument for fixed bias. Also fixed bias is necessary if the driving amplitude varies, otherwise the circuit resonances will be shifted by self-bias variations so that the amplitude changes are compounded in some nonlinear manner.

      d. <u>Projected Capabilities</u>. The upper curve of Figure 9 is a plot of the optimum efficiencies of Figure 5 vs the ratio of fundamental frequency to diode cutoff frequency. Capacity diodes with cutoff frequencies greater than 100 K mc are now being made. If this value is assumed, it means that doubling efficiencies of 96% for 100 - 200 mc and 68% for 1,000 - 2,000 mc are forthcoming. The two lower curves were developed by accumulating both the efficiencies of the solid curve at octaves and coupling losses and thus indicate what may be expected when doublers are cascaded from a frequency of f/f_b = .001. This suggests the future possibility of developing say 10 watts of power at 100 mc from a transistor, applying this to cascaded optimum doublers with 100 K mc cutoff frequency diodes and 90% coupling efficiency for each, and deriving an output of 3.6 watts at 800 mc, 1.8 watts at 1,600 mc, etc.

2. Higher Harmonics

      For generation of harmonics higher than second within a single capacity diode it is found necessary to allow more than two sinusoidal currents to flow. With this added complexity, it is convenient to set up a table of the current components, charge components, and pertinent voltage components assuming the model diode of equation (2). Following is such a table for frequency tripling where (C1) means cos 1ωt and ... are terms which do not involve power.
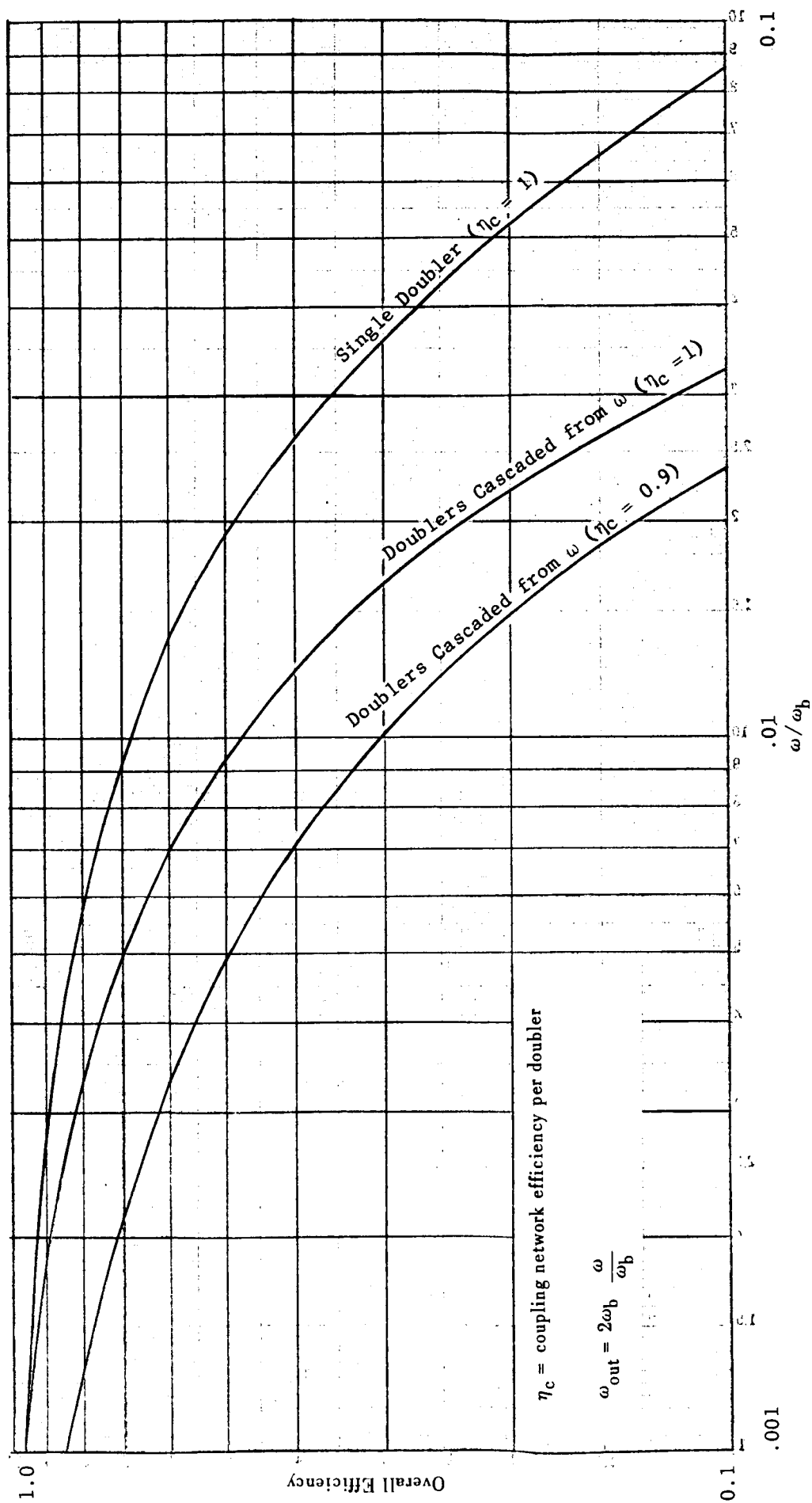
FIG. 9. EFFICIENCY OF CASCADED OPTIMUM DOUBLERS
VS
INPUT AND DIODE CUTOFF FREQUENCY AND COUPLING EFFICIENCY

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Frequency x 3:

i	q	$e' \times 4\,(\omega c_b)^2\, E_b$		
$I_1(C1)$	$\dfrac{I_1}{\omega}(S1)$	$\dfrac{-(I_1)^2}{2}(C2)$		
		$\dfrac{I_1 I_2}{2}(C1)$ $-\dfrac{I_1 I_2}{2}(C3)$		
$I_2(C2)$	$\dfrac{I_2}{2\omega}(S2)$	$\ldots (C4)$	$\dfrac{I_1 I_3}{3}(C2) \ldots (C4)$	
		$\dfrac{I_2 I_3}{6}(C1) \ldots (C5)$		
$I_3(C3)$	$\dfrac{I_3}{3\omega}(S3)$	$\ldots (C6)$		

From this table the average powers entering and leaving the diode may be easily written:

$$\frac{\overbrace{\dfrac{(I_1)^2 I_2}{2} + \dfrac{I_1 I_2 I_3}{6}}^{P'_{1\omega}} + \overbrace{\dfrac{I_1 I_2 I_3}{3} - \dfrac{(I_1)^2 I_2}{2}}^{P'_{2\omega}} - \overbrace{\dfrac{I_1 I_2 I_3}{2}}^{P'_{3\omega}}}{8(\omega c_b)^2\, E_b} = 0$$

The assumed currents have provided the desired function ($P'_{1\omega}$ is positive and $P'_{3\omega}$ is negative). $P'_{2\omega}$ should be made zero so that all fundamental power is converted to third harmonic power. This occurs when $I_3 = 3I_1/2$, so let:

$$i = I(C1) + mI(C2) + 3I/2(C3); \text{ so that } P'_{2\omega} = 0 \text{ and } e'_{2\omega} = 0$$

Then $P'_{1\omega} = P'_{3\omega} = P'$; the power handled within the diode:

$$P' = \frac{3m(I)^3}{16(\omega c_b)^2\, E_b}$$

and

$$P_{loss} = \left[(I)^2 + (mI)^2 + \left(\frac{3}{2}I\right)^2 \right] \frac{r}{2}$$

In a manner similar to the doubling example, efficiency and input and output impedances may be described in terms of power level, diode cutoff frequency and c_b and E_b constants. By experimenting with the shorthand table notation, the following tables of interest were found and still others may be determined by trial and error:

Frequency x 4:

i	q	$e' \times 4 \; (\omega c_b)^2 \; E_b$			
I(C1)	$\dfrac{I}{\omega}$ (S1)	$\dfrac{-(I)^2}{2}$ (C2)			
			$(I)^2$(C1) ...		
2I(C2)	$\dfrac{I}{\omega}$ (S2)	$\dfrac{-(I)^2}{2}$ (C4)		... ...	
		$\dfrac{(I)^2}{2}$ C2) ...			
2I(c4)	$\dfrac{I}{2\omega}$ (S4)	...			

Frequency x 8:

i	q	$e' \times 4 \; (\omega c_b)^2 \; E_b$			
I(C1)	$\dfrac{I}{\omega}$ (S1)	$-\dfrac{(I)^2}{2}$ (C2)			
			$(I)^2$(C1) ...		
2I(C2)	$\dfrac{I}{\omega}$ (S2)	$-\dfrac{(I)^2}{2}$ (C3)		... ...	
			$\dfrac{(I)^2}{2}$ (C2) ...		... ...
2I(C4)	$\dfrac{I}{2\omega}$ (S4)	$-\dfrac{(I)^2}{4}$ (C8)		... ...	
			$\dfrac{(I)^2}{2}$ (C4) ...		
8I(C8)	$\dfrac{I}{\omega}$ (C8)	...			

3. Parametric Mixers, Amplifiers and Oscillators

Let us consider the following table:

i	q	$e'\left[4(\omega c_b)^2\, E_b\right]$
$I_\omega \cos \omega t$	$\dfrac{I_\omega}{\omega} \sin \omega t$	...
$I_{(n-1)\omega} \cos(n-1)\omega t$	$\dfrac{I_{(n-1)\omega}}{(n-1)_\omega} \sin(n-1)\omega t$	$-\dfrac{I_\omega I_{(n-1)\omega}}{n-1}\cos n\omega t \;...$ $... \quad +\dfrac{I_\omega I_{n\omega}}{n}\cos(n-1)\omega t \;...$ $+\dfrac{I_{(n-1)\omega} I_{n\omega}}{n^2-n}\cos \omega t \;...$
$I_{n\omega} \cos n\,\omega t$	$\dfrac{I_{n\omega}}{n\omega} \sin n\,\omega t$	...

The number n may have any va..ue except these: n = -2; -1; -1/2; 0; 1/3; 1/2; 1; 2; 3 so that the omitted voltage terms in the table do not coincide with any of the three current frequencies to produce power. From this table the average powers entering and leaving the diode e' generator may be written:

$$\frac{I_\omega \, I_{(n-1)\omega}\, I_{n\omega}\,\left[\,\overbrace{1}^{P_\omega:} + \overbrace{(n-1)}^{P_{(n-1)\omega}:} - \overbrace{n}^{P_{n\omega}:}\,\right]}{8\,(n^2-n)\,(\omega c_b)^2\, E_b} = 0$$

The power at each frequency is indentified by the notation just above each term. One may quickly notice that the power at each frequency is proportional to that frequency. Therefore, if n is positive and greater than one, power is absorbed at ω and (n-1)ω and the sum of these powers is emitted at the sum frequency nω. If the (n-1)ω power comes from a local oscillator and the ω power is a signal, then the device is an up (frequency) converter with a signal output frequency of nω and has a signal conversion power gain of n, the frequency change ratio. If n is positive and less than one the same net result occurs because when n = 0.2 instead n = 5 (reciprocal) the same operation results except that the frequencies are then normalized with respect to the highest rather than the lowest. This amplifying up

converter is characterized by low noise (because it is reactive) and stable gain.

If in the preceding table I_ω is changed to $-I_\omega$ and this sign change is carried through, the powers entering and leaving the diode are reversed in sign. This may be seen most readily in the above summation of powers by substituting $-I_\omega$ for I_ω. It is then interesting to write the impedances of the e' generator at each frequency by taking the ratio of each voltage to current from the table with the sign change:

$$R_\omega = - \frac{I_{(n-1)\omega} \, I_{n\omega}}{I_\omega(n^2-n)} \times \frac{1}{4(\omega c_b)^2 E_b}$$

$$R_{(n-1)\omega} = - \frac{I_\omega I_{n\omega}}{I_{(n-1)\omega}(n)} \times \frac{1}{4(\omega c_b)^2 E_b}$$

$$R_{n\omega} = + \frac{I_\omega I_{(n-1)\omega}}{I_{n\omega}\,(n-1)} \times \frac{1}{4(\omega c_b)^2 E_b}$$

This shows that power may be absorbed at the $n\omega$ frequency and emitted at the other two frequencies. The circuit of Figure 10 will help visualize the situation.

The reactance poles and zeros specified in Figure 10 cause the current and resistance at each frequency terminal pair to equal the current and resistance of the e' generator at that frequency. To cause finite currents operation (three currents in this case) additional reactances are probably necessary to prevent other currents from flowing through the diode but these will be omitted here for simplicity. Let us examine the two negative resistances by writing their product:

$$R_\omega R_{(n-1)\omega} = \frac{(I_{n\omega})^2}{(n^3-n^2) \left[4(\omega c_b)^2 E_b \right]^2}$$

or

$$\sqrt{R_\omega R_{(n-1)\omega}} = \frac{I_{n\omega}}{\sqrt{n^3-n^2}\; 4(\omega c_b)^2 E_b}$$

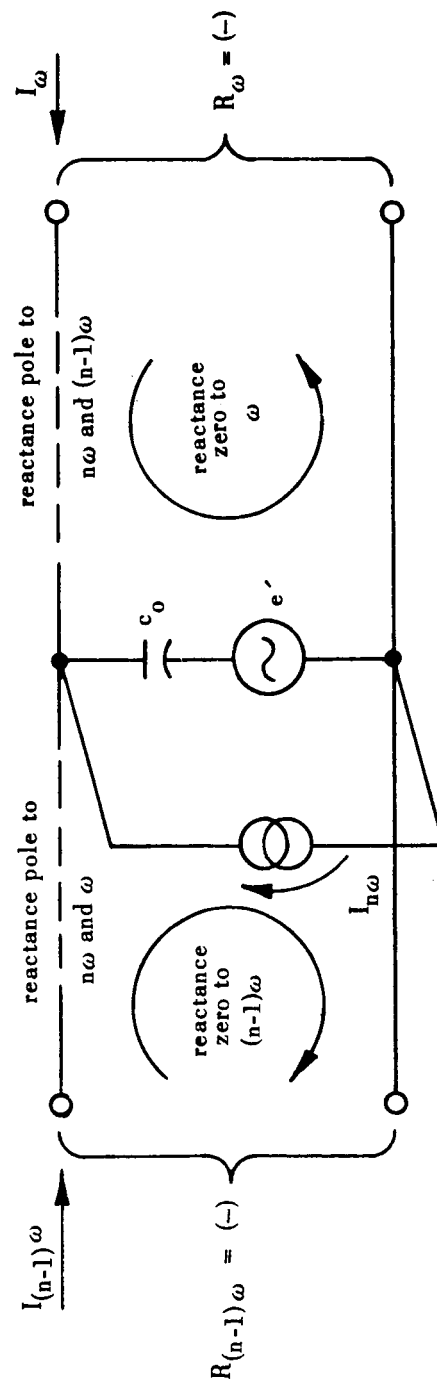This shows that the mean negative resistance is a constant determined

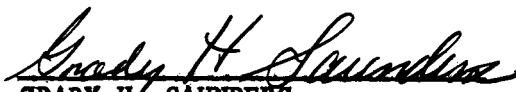FIG. 10. A THREE-BRANCH FINITE CURRENTS CIRCUIT

by the $I_{n\omega}$ (pump) current, the ratio of frequencies n, the lowest
frequency ω, and the diode constants. External positive resistances
will be connected to each pair of negative resistance terminals. If
then the net resistance in the ω and $(n-1)\omega$ loops is zero, the diode
will oscillate at ω and $(n-1)\omega$ and derive the power to oscillate from
the ω pump. This will occur when the external resistances have the
constant product written above for R_ω and $R_{(n-1)\omega}$. If the product of
the external resistances is greater, oscillation will not occur since
then there is not enough negative resistance generated to cancel the
positive resistance in the circuit. Under these circumstances the
circuit may be used as an amplifying up converter, an amplifying down
converter, or as a nonfrequency converting amplifier at either ω or
$(n-1)\omega$. In the first case, a portion of the gain is obtained from con-
verting up, as happened in the sum frequency up converter, but all of
these arrangements amplify because of the negative resistances generated.
For this reason it is possible for all of these to provide up to infinite
gain (oscillation). If the balance between negative and positive resist-
ance is made critical, for high gain the circuit is likely to break
into oscillation if small changes occur in pump current or in either of
the external circuits connected to the ω or $(n-1)\omega$ terminals. These
negative resistance applications are characterized by low noise because
they are reactive; and by high selectivity, high gain, and poor gain
stability because of the negative resistance. It would seem that super-
regenerative techniques could be applied to advantage in such devices.
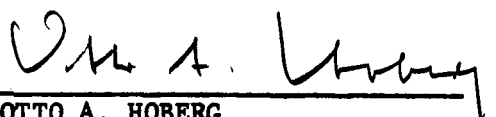Also, the devices should should make good low noise oscillators.
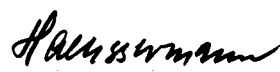
4. Subharmonic Generation

If a capacity diode is operated as an oscillator as described
above and n is chosen to be an integer, the ω oscillations will syn-
chronize with the $n\omega$ pump signal so that ω is a subharmonic of the $n\omega$
input. Thus, capacity diodes as frequency dividers are in reality
oscillating parametric mixers with three frequencies of current neces-
sary to the operation. One apparent exception to this is the frequency
halver which requires current at only ω and 2ω, but this happens only
because two of the three frequencies required happen to coincide in
this special case.

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